SIGMA BASICS

JUNE 1968

(Revision I)

FOR TRAINING PURPOSES ONLY

SDS SCIENTIFIC DATA SYSTEMS TECHNICAL TRAINING SECTION

MT-CH-Σ-1

PREFACE

The development of the Sigma Product Line resulted in the generation of a huge mass of supporting documentation. This training document is an attempt to combine information from many different documents which pertain to the understanding and maintenance of all Sigma products. It is also an attempt to supply explanations and carifications on the interpretation and use of these documents; explanations which are not presently found elsewhere.

This document is aimed at giving the user the basic knowledge of Sigma hardware structures so that he can assume the study of specific Sigma equipment armed with a solid background of the fundamental principles involved in the operation of any Sigma device.

This document assumes that the reader is thoroughly familiar with digital electronic circuitry and Boolean algebra. Experience on other digital computers will allow the reader to assimilate some of the information easier, however, it is not a prerequisite.

Our appreciation is extended to Robert J. Spinrad, Vice-President of Programming, for his permission to include his excellent article on software, written while he was a member of the Brookhaven National Laboratory Staff.

SCIENTIFIC DATA SYSTEMS
TECHNICAL TRAINING STAFF

TABLE OF CONTENTS

WHAT IS SIGMA?

SECTION I

WHAT IS SIGMA?

In March 1966, SDS announced Sigma 7, marking the eigth introduction by SDS of a computer offering greater capability and reliability than competitively priced machines.

The success of the Sigma line since then underscores the company's ability to develop advanced equipment by devising and putting into practice new development techniques such as:

* Critical-path charting methods in the design, programming, manufacturing, and documentation efforts to insure on-time delivery;
* Extensive use of standardized elements to make up the computer system, thereby minimzing manufacturing costs;
* Special computer programs to expedite the design of integrated circuits and computer logic;
* Automated logic implementation, including logic equations, wire lists, and wire verification, to speed the manufacturing process, and;
* Computer-controlled and semi-automatic testing methods at every level of assembly to insure maximum interface efficiency and customer satisfaction.

The specific techniques that led to the development of the Sigma 7 were established several years ago when SDS engineers saw that new developments in computer technology made possible radically new approaches in design.

Therefore, in undertaking a new computer development program, SDS planners set themselves these goals:

* To use the most advanced techniques that would be economically feasible by the time manufacturing began;
* To meet the needs of the users by looking ahead to the time when the new computers would be coming into use;
* To integrate hardware with software in a fully coordinated design that would offer more computation per dollar, and;
* To make both hardware and software modular and expandible to satisfy a wide range of requirements.

The result, announced two years later, was Sigma 7, first in a family of third-generation SDS computers. Sigma 7 is a fast, medium-size computer system that can simutaneously control real-time operations, interact with a large number of time-shared user stations, solve scientific problems, and process business data.

Sigma 7 was followed by Sigma 2, a small, low-cost computer system, in August 1966. Sigma 5 was then announced in the spring of 1967 as a fast, medium-size system which filled the capability and application gap between the Sigma 2 and Sigma 7.

Along with the three computer systems, SDS announced the availibility of many Sigma peripheral devices such as Card Readers and Punches, Teletypes, Line Printers, RAD Files, Magnetic Tape Transports, Paper Tape Systems, Keyboard Displays, and Communications equipment.

Other devices were concurrently announced which operate with a Sigma computer, such as D-A Converters, Multiplexors, and other Systems devices.

The Sigma Product Line is far from completed. Other computers will be announced, as well as peripherals, as the market dictates. Plans are in progress to create a computer system which fills the gap between the Sigma 2 and Sigma 5 computers. Many of the Sigma 5 and 7 computers are being shipped as a multi-processor computer system, therefore, designers are looking ahead to the design of a fully integrated multi-processor computer system to more fully meet the needs of that market.

When the Sigma Product Line is completed it should represent a formidable array of computer hardware and software systems which can effectively compete in any computer system environment.

Sigma is a state-of-the-art computer system. Techniques and methods developed for Sigma will be with the industry for many years to come, even in an industry noted for its changing technology.

Therefore, the knowledge you will be gaining in the Sigma courses you are entering will be invaluable in your immediate needs, and profitable in your long-range career goals. Keep this in mind as you attend the training here at SDS in the Sigma Product Line equipment, and devote all of your energy to learning. Knowledge is a very salable and indispensable part of your career; appreciate the opportunity, and take advantage of it.

SIGMA PRODUCT LINE

SECTION II

THE SIGMA PRODUCT LINE

SIGMA 2

Model Number	Description
8001	Sigma 2 Central Processor Unit
8011	2 Real Time Clocks
8012	Memory Parity Interrupt
8013	Power Fail Safe
8014	Protection Feature
8020	Multiply/Divide Option
8021	Interrupt Control Chassis
8022	Priority Interrupts, 2 levels
8023	Integral Priority Interrupts, 2 levels
8050	External Memory Adapter, Model II
8051	Basic Core Memory, 4096 words
8053	Memory Increment, 4096 words
8054	External Memory Adapter, Model I
8055	Memory 2-Way Access
8070	External Interface Feature
8071	Additional 4 I/O Channels
8072	Watchdog Timer
8091	Integral KSR Teletype
8092	Integral ASR Teletype

SIGMA 5

Model Number	Description
8201	Sigma 5 Central Processor Unit
8202	Sigma 5 Central Processor Unit without Integral IOP
8203	Integral IOP
8211	2 Additional Real Time Clocks
8213	Power Fail Safe
8214	Memory Protect
8216	Additional Register Block (16 General Purpose Registers)
8218	Floating Point Arithmetic Unit
8221	Interrupt Control Chassis (16 Priority Interrupt levels)
8222	Priority Interrupts, 2 levels
8251	Basic Core Memory, 4096 words
8252	Memory Increment, 4096 words
8255	Memory 2-Way Access
8256	Memory 3-Way Access
8257	Memory 6-Way Access
8270	External Interface Feature
8271	Multiplexor I/O Processor with 8 Channels
8272	Additional 8 Channels for MIOP
8285	Selector I/O Processor, Model II
8291	CFE-3 Control Unit
8292	2 CFE-3 Multiply/Add Units

SIGMA 7

Model Number	Description
8401	Sigma 7 Central Processor Unit
8411	2 Additional Real Time Clocks
8413	Power Fail Safe
8414	Memory Write Protection
8415	Memory Map and Access Protection
8416	Additional Register Block (16 General Purpose Registers)
8418	Floating Point Arithmetic
8419	Decimal Arithmetic Unit
8421	Interrupt Control Chassis (16 Priority Interrupt levels)
8422	Priority Interrupts, 2 levels
8451	Basic Core Memory, 4096 words
8452	Memory Increment, 4096 words
8456	Memory 3-Way Access
8457	Memory 6-Way Access
8471	Multiplexor I/O Processor with 8 Channels
8472	Additional 8 Channels for MIOP
8485	Selector I/O Processor, Model II
8491	CFE-3 Control Unit
8492	2 CFE-3 Multiply/Add Units
8495	System Supervisory Console (Free-Standing)

SIGMA PERIPHERAL DEVICES

Model Number	Description
7010	KSR Teletype with Controller, 10CPS
7011	KSR Teletype without Controller, 10CPS
7014	KSR Teletype without Sigma 2 Integral Controller, 10CPS
7020	ASR Teletype with Controller, 10CPS
7021	ASR Teletype without Controller, 10CPS
7060	Paper Tape System with Controller and Rack (Reader, Punch, and Spooler).
7061	Paper Tape System Cabinet and Controller
7062	Paper Tape Reader, 300CPS
7063	Paper Tape Punch, 120CPS
7064	Paper Tape Spooler
7120	Card Reader, 400CPM
7140	Card Reader, 1500CPM
7160	Card Punch, 300CPM
7201	RAD Controller
7202	RAD Storage Unit, .75MB; 188,000 bytes/second
7204	RAD Storage Unit, 3.0MB; 188,000 bytes/second
7321	Magnetic Tape Controller
7322	60KB Magnetic Tape Station (75 IPS, 9-Track)
7323	120KB Magnetic Tape Station (150IPS, 9-Track)
7361	20KC Magnetic Tape Controller
7362	20KC Magnetic Tape Station (37.5 IPS, 7-Track)
7365	BCD Option
7371	Magnetic Tape Controller
7372	60KC Magnetic Tape Station (75 IPS, 7-Track)
7374	Binary Packing Option

7440	Buffered Line Printer, 600LPM
7445	Buffered Line Printer, 1000LPM
7530	Graph Plotter (11 Inch)
7531	Graph Plotter (30 Inch)
7550	Keyboard Display, Model I
7551	Message Mode Feature
7553	Hard Copy Output Feature
7555	Keyboard Display, Model II
7556	High Speed Transmission Feature
7601	Data Set Controller
7602	Full Duplex Feature
7603	Automatic Dialling Feature
7611	Communications Controller
7612	Format Group Timing Unit
7613	Line Interface Unit
7614	High Speed Feature
7615	Send Module
7616	Receive Module
7617	DC Telegraph Interface
7618	Automatic Dialing Unit
7619	Additional Dialing Position
7650	Channel Interface Unit
7700	Inter-processor Interrupt Feature
7710	Direct I/O Bus-Sharing Adapter
7720	Multi-Controller Peripheral Switch
7721	Manual Control for Peripheral Switch

SYSTEMS INTERFACE UNITS

Model Number	Description
7900	Device Subcontroller
7901	Peripheral Equipment Tester
7910	Analog Output Controller
7914	Analog Input Controller
7922	Analog and Digital Adapter
7929	IOP to DIO Adapter
7920	DIO Adapter
7931	DIO Adapter Expander
7950	8 Stored Digital Outputs
7951	16 Digital Inputs
7952	8 Pulsed Digital Outputs (Quiescent +4 VDC)
7953	8 Pulsed Digital Outputs (Quiescent 0 VDC)
7954	8 Relay/Lamp Drivers
7969	Frequency Control Basic
7970	Frequency Source Unit, Manual
7971	Program Control Basic
7972	Frequency Source Unit, Programmed

ACCESSORIES

Model Number	Description
8901	Cabinet Side Panel
8902	Front Door
8905	Utility Table
8910	19" Sigma Basic Cabinet
8920	24" Sigma Basic Cabinet

"T" SERIES LOGIC MODULES

SECTION III

T SERIES LOGIC MODULES

Experience with the successful SDS Sigma computers has shown that at the present state of component development the best performance, coupled with lower costs, is obtained when monolithic DTL (Diode-Transistor Logic) integrated circuit flip-flops, inverters, and buffer amplifiers are combined with close tolerance, discrete diode-resistor gates and output pull-up resistors.

Integrated circuits cut costs, save space, improve reliability, and improve performance, by replacing repetitive clusters of transistor circuitry.

Diode gates retain flexibility where needed, in the gating structures, and help provide a very high noise rejection of 1.5 volts.

Discrete pull-up resistors (resistors connected between the output transistor and the DC voltage supply) allow the use of high current drive by keeping most power dissipation outside the IC package.

High current drive makes fan-out large, up to 14 gates per output, and easily permits use of clock frequencies up to 10 Mhz because logic line capacitance can be charged quickly.

All of these circuits are placed on the same size epoxy-glass etched circuit card, 4.5 inches high by 4.75 inches deep. The card has 52 gold-plated connector contacts to maintain circuit accessibility and still provide dense packing.

The cards plug into connectors which have reliable gold-plated, spring-loaded, bifurcated (2-pronged) contacts. Thirty-two modules can be placed side-by-side in 19" wide mounting cases, which are available in a wide variety of fixed-mount and hinged models having either wire-wrap or solder tail back panel pins.

Each mounting case incorporates a ground plane for noise immunity, and includes built-in voltage buses. Ninety-module tilting drawer cases are also offered. Any of the cases can be mounted in one of two types of cabinets which have 19" RETMA rails, doors, AC power wiring, swing-out frames, and optional side panels. a 300 cfm blower is available for cooling. An extender card is provided for troubleshooting.

Jumper wire kits, spooled wire, and wiring tools are available to further simplify mechanical assembly. Blank cards and drilled breadboards with circuit etch are also available.

Further wiring information can be obtained in Section V.

GENERAL SPECIFICATIONS

SUPPLY VOLTAGES

+4 VDC, $\pm$ 10%
+8 VDC, $\pm$ 10%
-8 VDC, $\pm$ 10%

LOGIC LEVELS

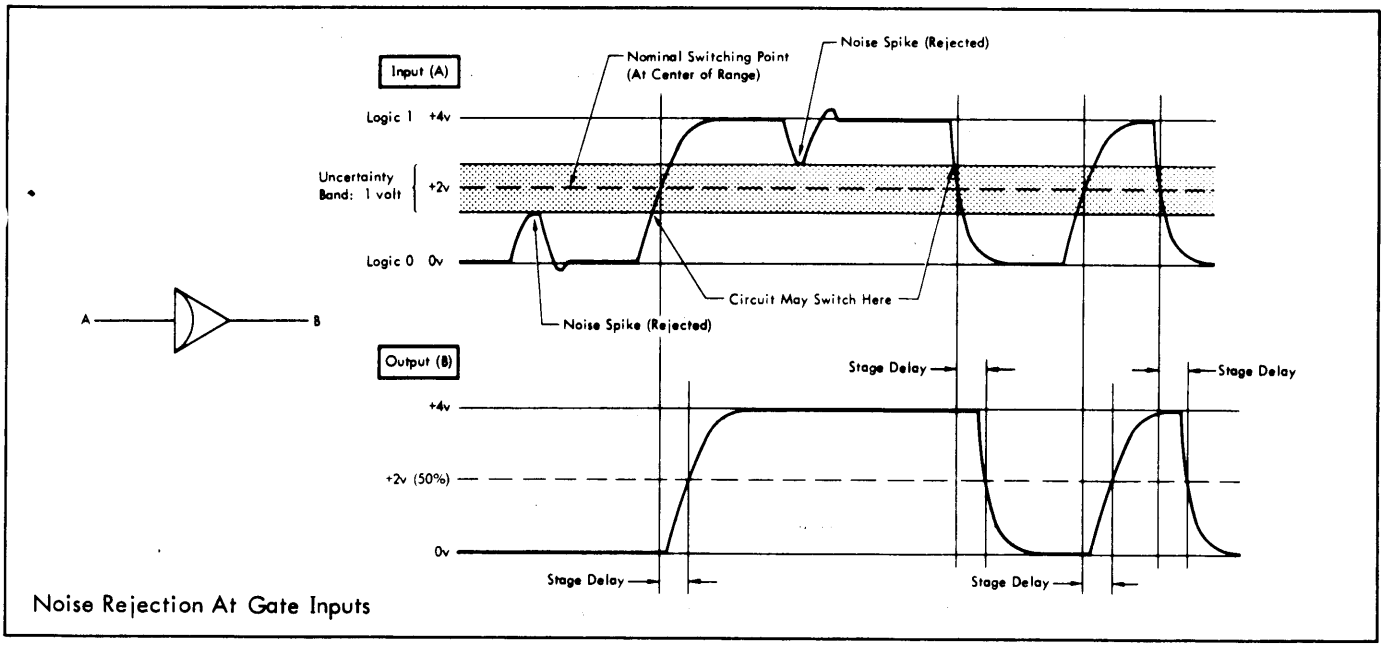
LOGIC "1": +4 VDC, nominal; +3.6 VDC to +10 VDC acceptable as inputs.
+3.6 VDC to +4.4 VDC maximum output variation.

LOGIC "0": 0 VDC nominal; +1.0 to -3 VDC acceptable as inputs.
0 VDC to +0.5 VDC maximum output variation.

NOISE THRESHOLDS

At Logic "0" - +1.5 VDC (greater may trigger True)

At Logic "1" - +2.5 VDC (lower may trigger False)



Noise Rejection At Gate Inputs

LOADING

1 Unit fan-out load is defined as 3.8 ma max., at the conducting logic level (0 VDC).

Input Loading: Any logic input applies 1 Unit Load to the preceding signal source, unless otherwise noted.

Output Loading: Buffer Amplifier, inverter amplifier, or one flip-flop output can drive 14 unit loads. (One flip-flop can be said to drive 28 unit loads, 14 for each output).
When buffer, inverter, or flip-flop outputs are wired together to form a wired logic function, each output attached to the node absorbs 2 unit loads due to the additional pull-up resistor placed at the node.

TIMING

Stage Delay:	Typical	Worst-case
Buffered gate	18 nsec	30 nsec
Flip-Flop	40 nsec	60 nsec

Frequency Range of Clock: DC to 10 Mhz

Minimum Input Timing: Flip-Flop DC inputs (Set or Reset) must be true for at least 40 nsec. AC Inputs (Set or Reset) must be true for 30 nsec. before clock changes from true to false, and 5 nsec thereafter.

Minimum Clock Duration: Clock must be true for 30 nsec., false for 60 nsec. Triggering takes place on falling edge when clock reaches +2 VDC (nominal) switching point.

TEMPERATURE

Ambient Operating Temperature: 5'C to 71 C (41'F to 160'F)

Storage Temperature: -55'C to +150'C

Further loading and wiring information can be found in Section V.

INTEGRATED CIRCUIT BUILDING BLOCKS

Only 6 basic IC components are used throughout the entire T Series Logic Module line to implement the various active circuits. They are:

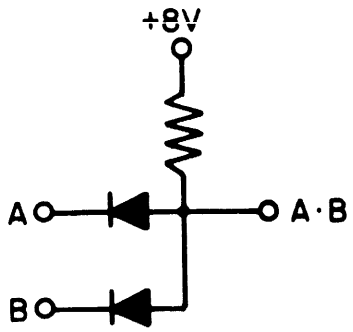
SDS Number	Description
304	8-bit Memory Element
305	Inverting Amplifier
306	Buffer Amplifier
307	Flip-Flop
308	Discriminator
311	Flip-Flop with Delay Control

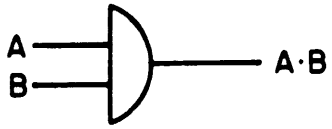
SDS is currently producing a seventh IC circuit, the SDS 309 Buffer Latch, which will be used on newly-designed equipment. No information is available at this time on the SDS 309.

IC Diode-Resistor Gating

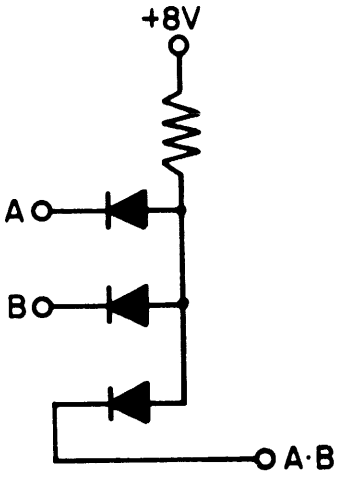
All IC components utilize external diode-resistor input gating when required. The diodes are 1N4154 Silicon diodes, and the gate load resistors are typically 2.2K-ohm, ± 5%, ¼-watt film resistors, returned to the +8 VDC power supply voltage. The gating structures are of three types: logical AND, OR, and a logical AND/OR combination:

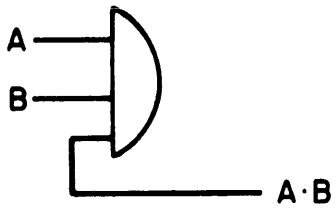
LOGICAL-AND - NO ISOLATION



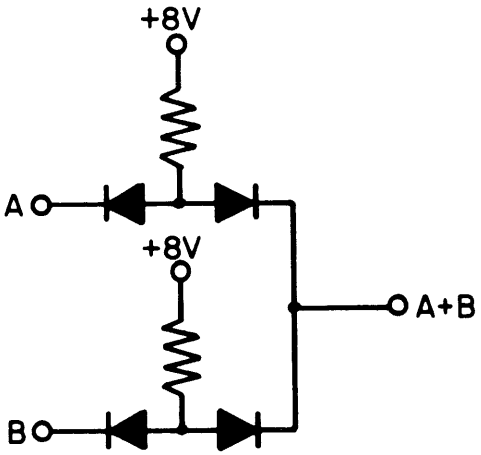


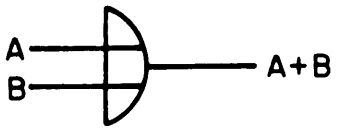
LOGICAL-AND - WITH ISOLATION



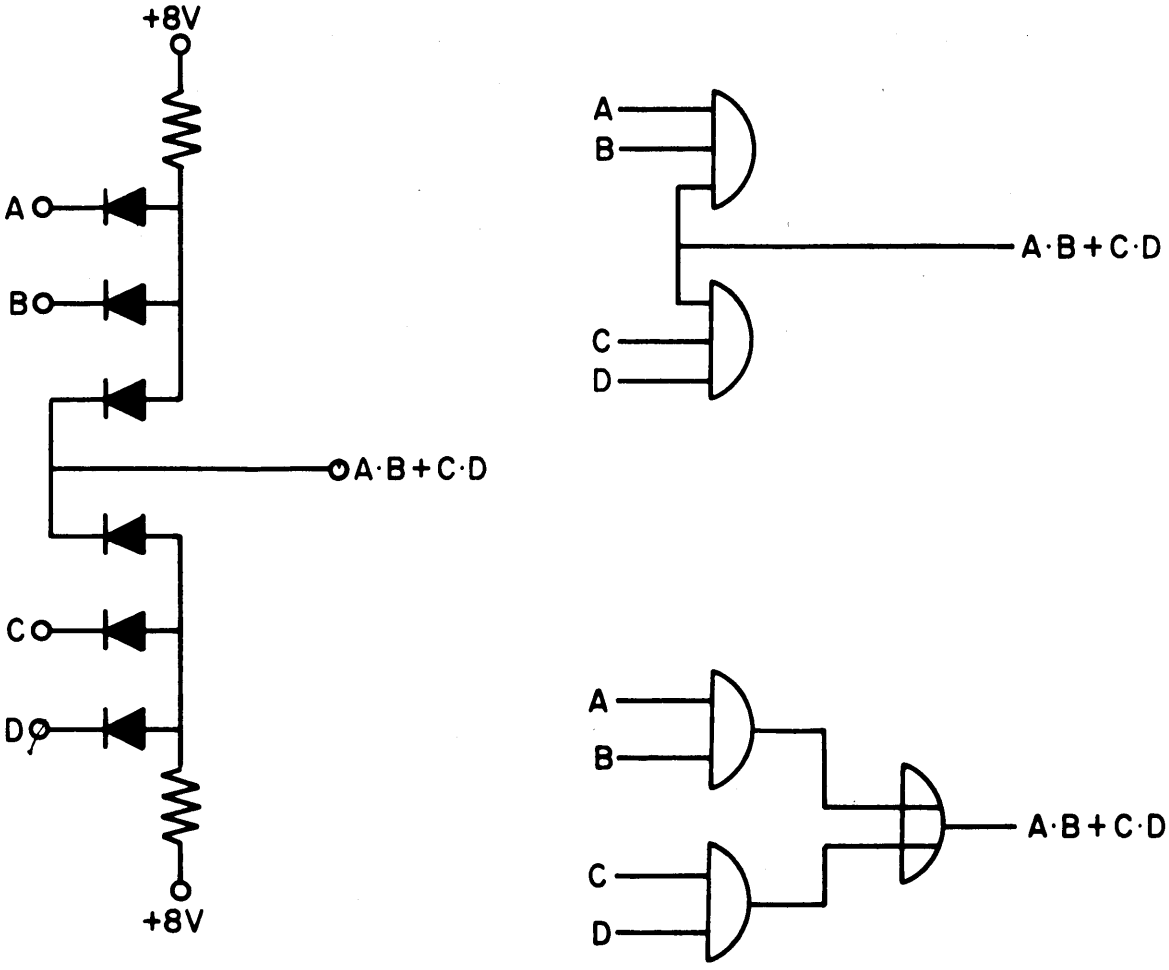


LOGICAL-OR





LOGICAL - AND/OR COMBINATION

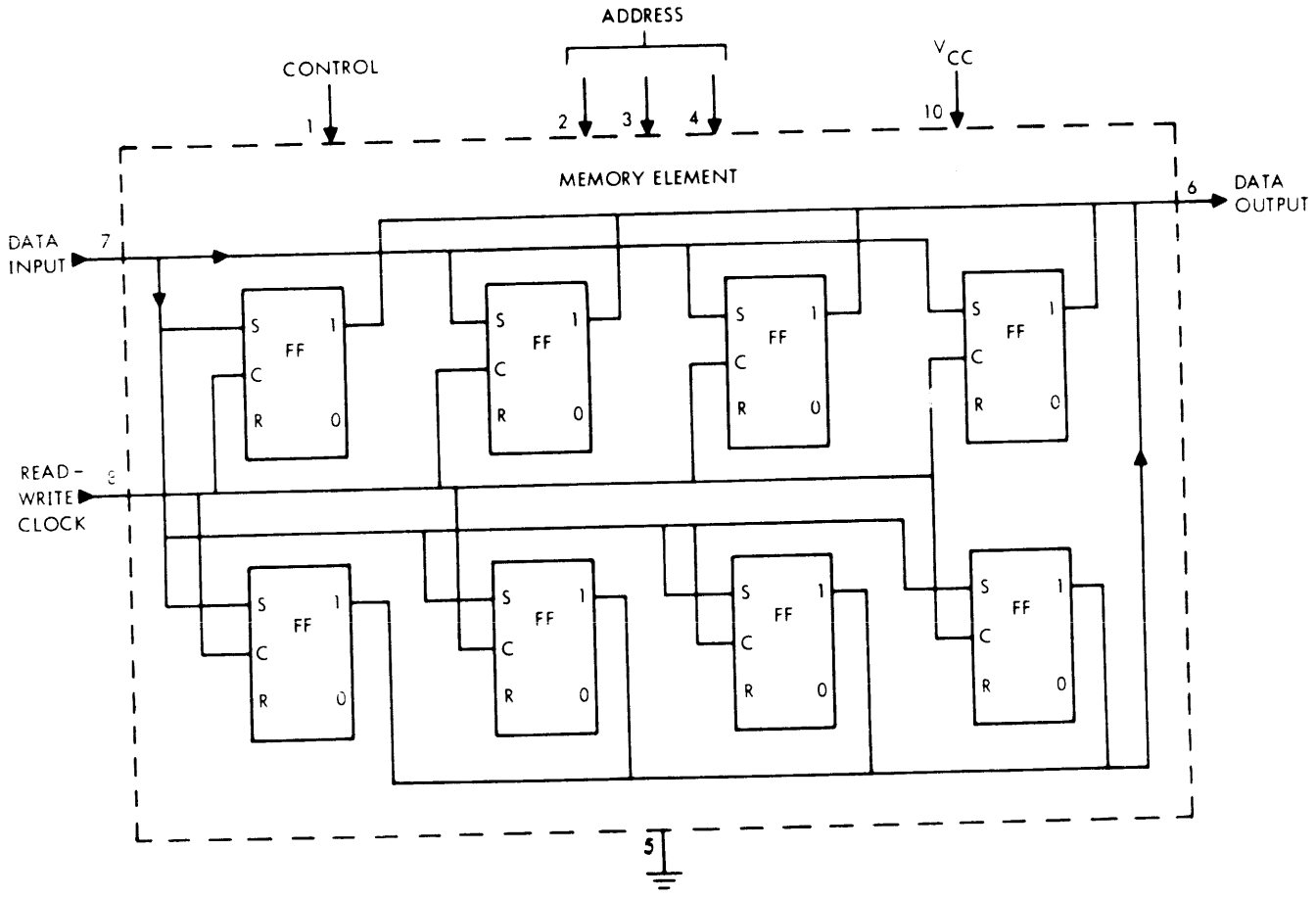


Note: either symbolic form is correct; the top is preferred.

SDS 304 8-BIT MEMORY ELEMENT

The SDS 304 Memory Element is the heart of what are referred to as "Fast-Access" or "Scratchpad" memory. This Memory Element consists of 8 bistable multivibrators, control logic, 3-bit address decode logic, and input/output logic within a 10-lead TO-5 can. The circuit is fabricated as a semiconductor monolithic integrated circuit. Each Memory Element can be thought of as 8, 1-bit registers, each register being uniquely addressed by a 3-bit address.

SIMPLIFIED LOGIC DIAGRAM



SDS 304 Memory Element, Simplified Diagram

THEORY OF OPERATION

The Control Line (pin 1) enables the Memory Element to be either sensed or changed, and is usually a function of another address bit. When this line is +4 VDC, data can be "read" on pin 6 from the flip-flop currently being addressed by the Address Lines, pins 2, 3, & 4.

If the Read/Write Clock (pin 8) Line is also at +4 VDC, the flip-flop currently being addressed will assume the state of the Data Input Line (pin 7).

If the Data Input Line is at +4 VDC, the currently addressed flip-flop will Set. If the Data Input Line is at 0 VDC, the currently addressed flip-flop will Reset. This action occurs only if the Read/Write Clock Line is at +4 VDC.

Therefore, to "read" from the Memory Element, the Control Line must be at +4 VDC, and the Address Lines will be decoded to select the unique flip-flop to be read.

To change a flip-flop within the Memory Element, the Control Line and the Read/Write Clock must be at +4 VDC. The uniquely addressed flip-flop will then assume the state of the Data Input Line.

The Memory Element is volatile since the removal of DC power will destroy the contents of the 8, 1-bit registers. When power is applied, the 8 flip-flops may assume either a Set or Reset condition.

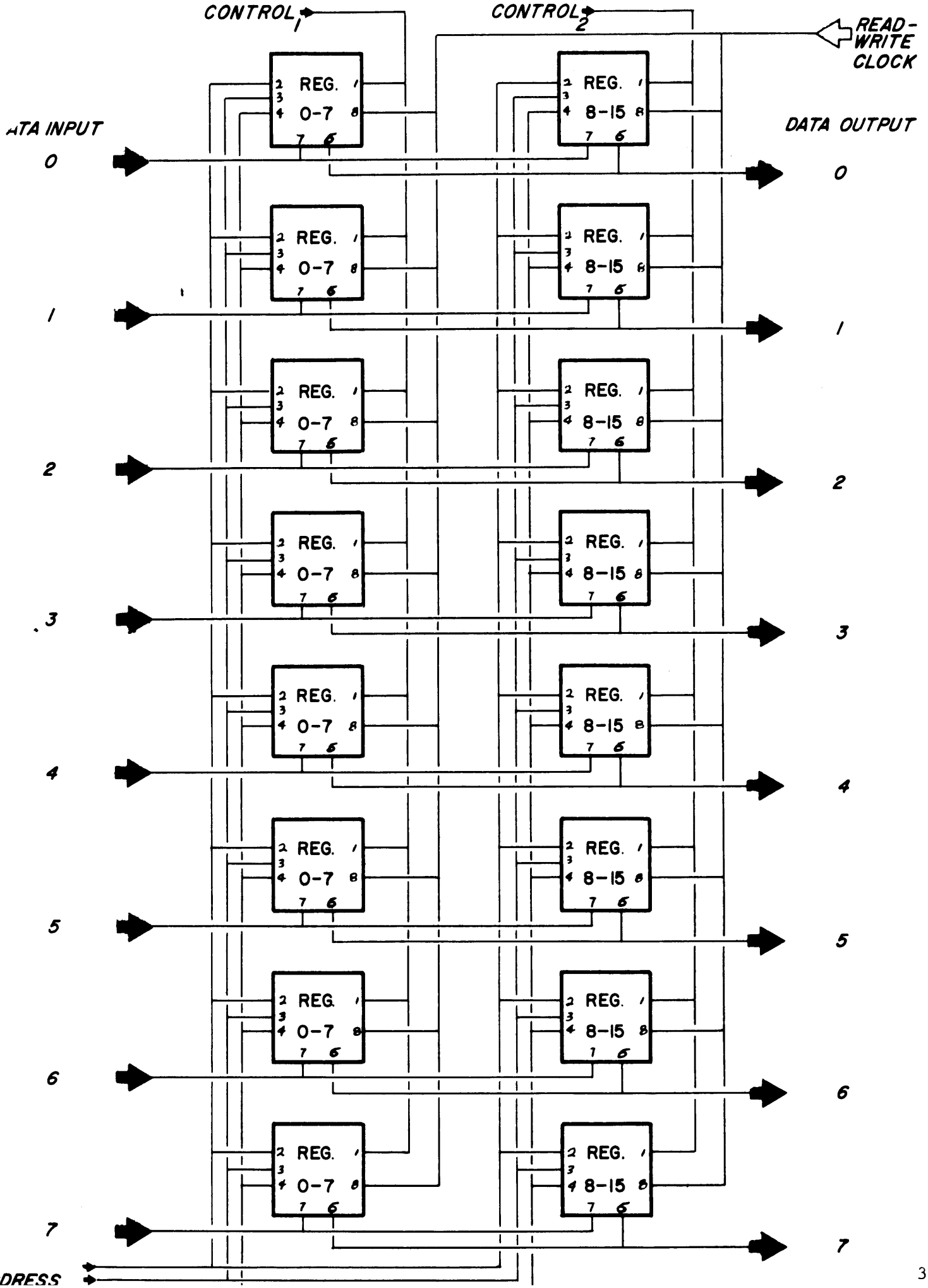
APPLICATION

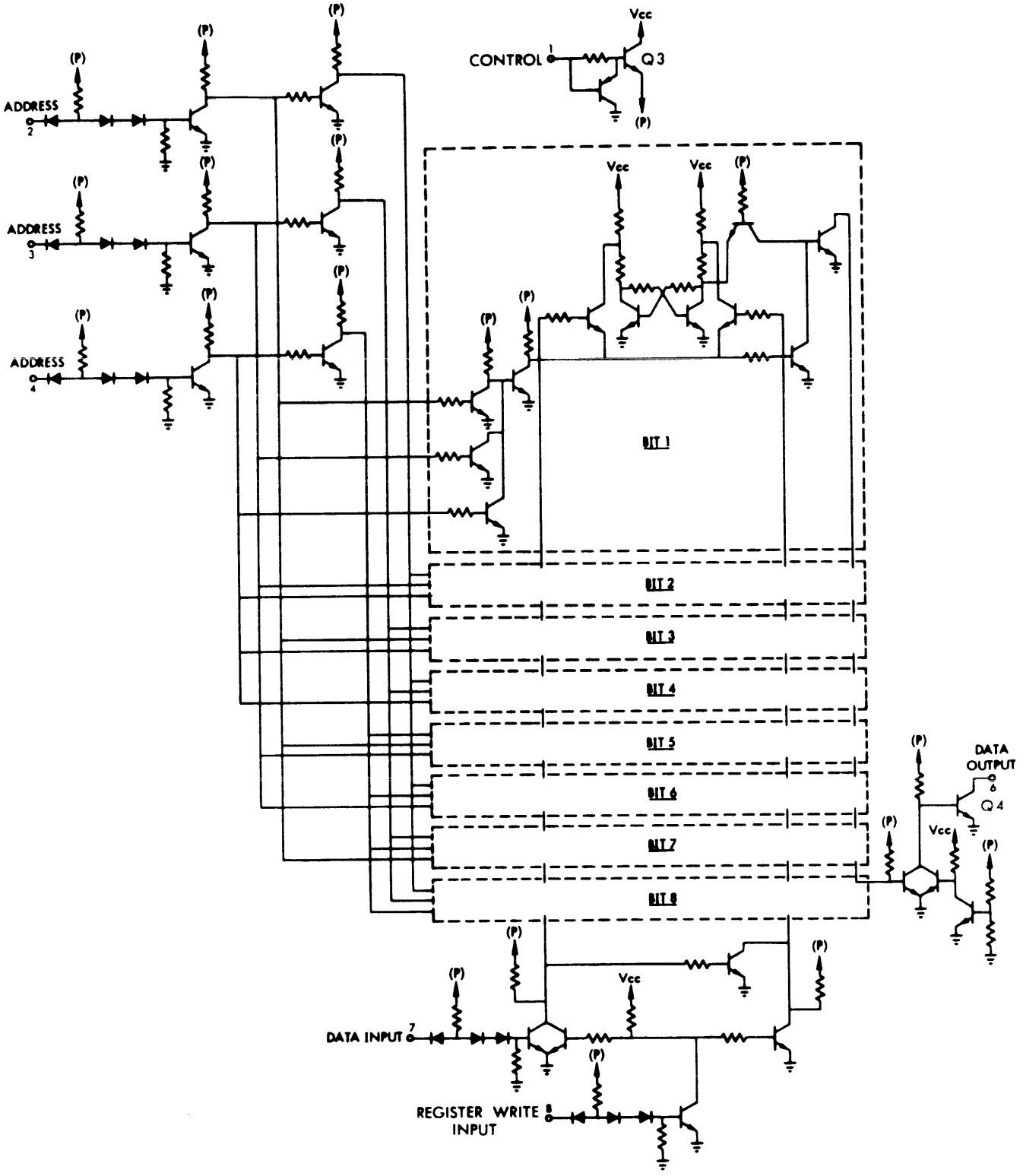
The SDS 304 is implemented to form "Fast-Access" registers of various lengths, and never as a stand-alone flip-flop. The diagram on the next page represents how 16 of the SDS 304 Memory Elements are used to form 16 8-bit registers which can operate with parallel input/output data.

In this application, the Control Lines are common to eight SDS 304 Memory Elements, and are controlled by the most significant address bit of a 4-bit address field. The 3 least significant bits of the address field are common to all 16 of the Memory Elements. Control Line 1 is equal to the address binary weight of $2^{\overline{3}}$, and Control Line 2 is equal to 2^3. Pin 2 of all cans is equal to the binary weight 2^2; pin 3 of all cans is equal to 2^1, and pin 4 of all cans is equal to 2^0. Thus, when the address field is equal to 0000, Control Line 1 will be true, and will enable the left-hand set of cans. The address lines, pins 2, 3, & 4 will then select one flip-flop from each of these 8 cans, allowing 8 bits of data to be read from pin 5 of these 8 cans in parallel.

The Data Output Lines (pin 6) of the left-hand set of cans are tied to the same lines from the right-hand set of cans, forming a wired "AND". All unselected cans will have a "1" output.

As the address field changes through its 4-bit structure, it can be seen that addresses in the range 0000 through 0111 will cause data to be accessed from the left-hand set of cans since Control Line 1 will be true. Thus, the left-hand set of cans could be referred to as registers 0-7. When the address swings into the range 1000 through 1111, Control Line 2 will be true, and the right-hand set of cans will be accessed. These could then be referred to as registers 8-15.


CONTROL 1
CONTROL 2
READ-WRITE CLOCK
ATA INPUT
DATA OUTPUT
REG. 0-7
REG. 8-15
0
1
2
3
4
5
6
7
ADDRESS

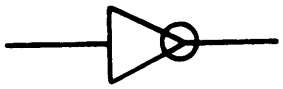


SDS304 Memory Element Schematic Diagram

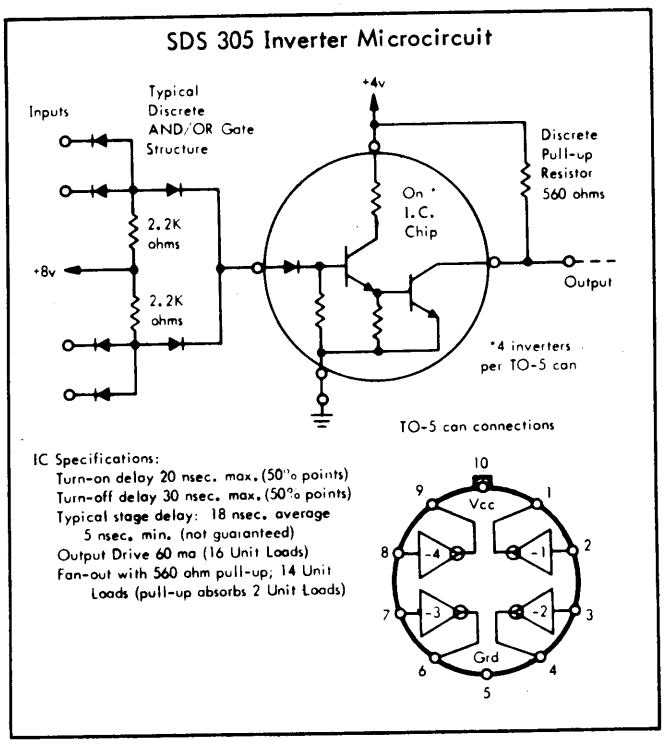
SDS 305 INVERTER

The SDS 305 contains 4 microcircuit Inverter Amplifiers housed in a 10-lead TO-5 can. The circuit is fabricated as a semiconductor monolithic integrated circuit. Each Inverter circuit presents the logical inversion of the input signal at the output. The Inverters will drive, and must be driven by, diode-resistor AND/OR gates.

LOGIC SYMBOL (1 of 4)



INPUT	OUTPUT
0 VDC	+4 VDC
+4 VDC	0 VDC
OPEN	0 VDC

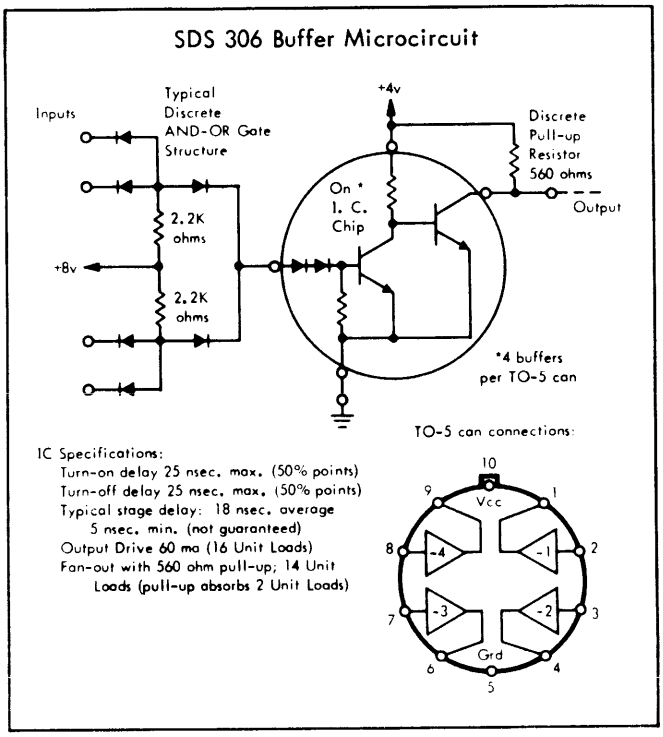


SDS 306 BUFFER

The SDS 306 contains 4 microcircuit Buffer Amplifiers housed in a 10-lead TO-5 can. The circuit is fabricated as a semiconductor monolithic integrated circuit. Each Buffer presents the logical equivalent of the input signal at the output, current-amplified. The Buffer will drive, and must be driven by, diode-resistor AND/OR gates.

LOGIC SYMBOL (1 of 4)

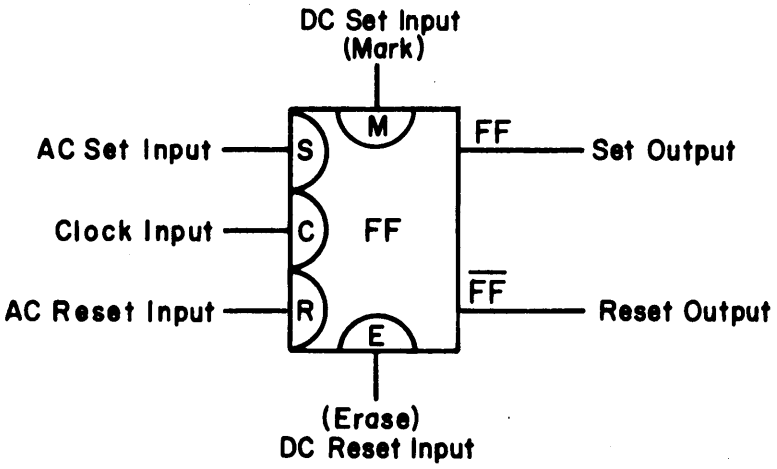
INPUT	OUTPUT
+ 4 VDC	+4 VDC
0 VDC	0 VDC
OPEN	+4 VDC



SDS 307 FLIP-FLOP

The SDS 307 is a microcircuit flip-flop housed in a 10-lead TO-5 can. The circuit is fabricated as a semiconductor monolithic integrated circuit. The SDS 307 is capable of being used as a DC flip-flop (no clock), an AC flip-flop (clocked), or both.

LOGIC SYMBOL

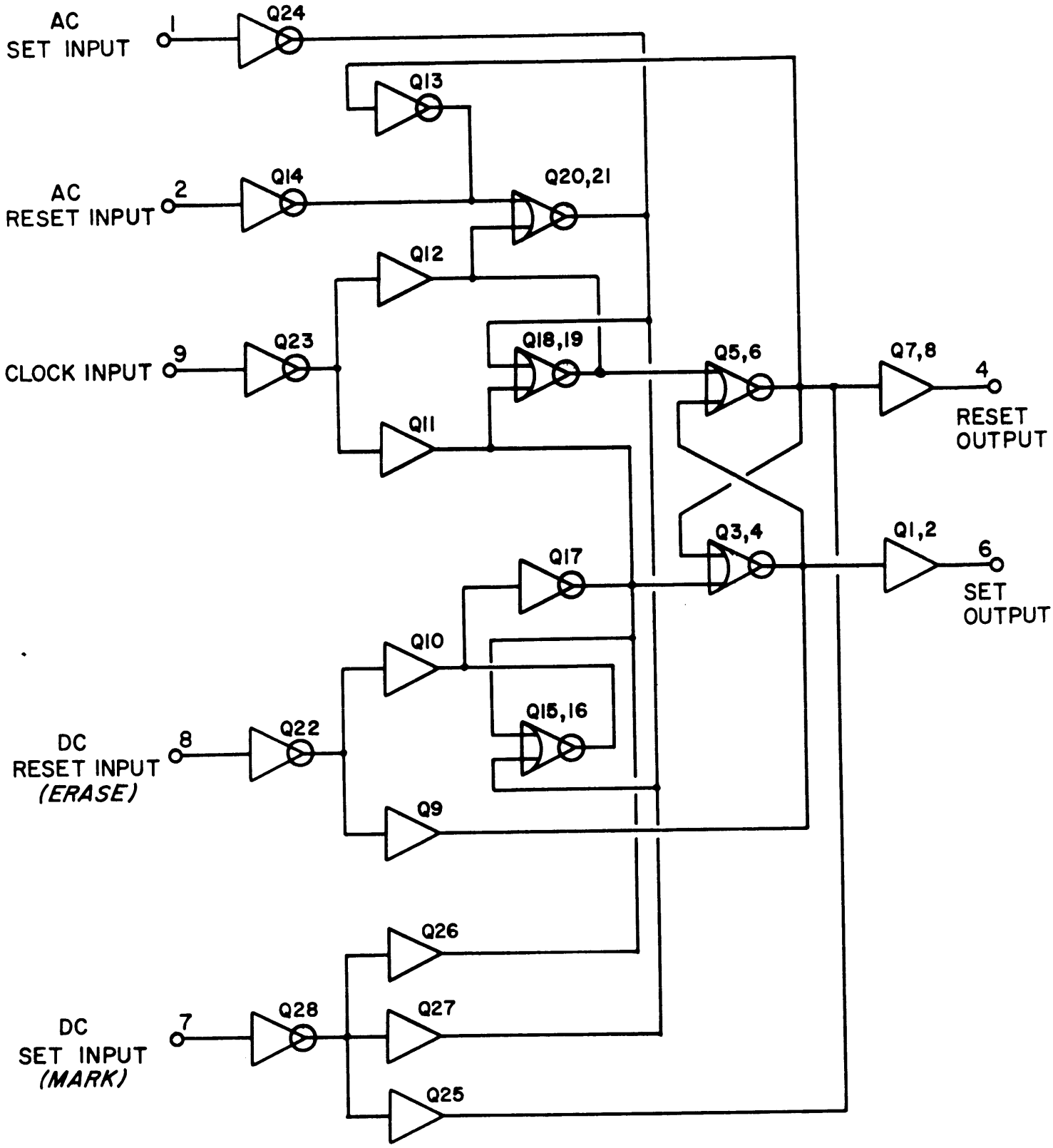


CIRCUIT DESCRIPTION

The operation can best be described by the logic diagram shown on the next page, which breaks the flip-flop into various subcircuits. The circuitry consists of 28 transistors, 36 resistors, and 10 diodes.

As can be seen from the logic diagram, the flip-flop is essentially a structure of NOR elements.

The flip-flop has a pair of DC inputs (called MARK for DC Set Input and ERASE for DC Reset Input. MARK is also referred in the equations as the FORCE input.) which can be used to make the flip-flop behave like a simple DC flip-flop. Their primary use is to override the AC Set and Reset Inputs, so that the flip-flop can be preset or cleared between clock trailing edges.



SIMPLIFIED LOGIC DIAGRAM, SDS 307

When the MARK input becomes True, the Set Output becomes True and stays True regardless of the state of the MARK input, and the Reset Output becomes False. When the ERASE input becomes True, the Reset Output becomes True and stays True, and the Set Output becomes False. If both DC inputs become True simultaneously, both Set and Reset Outputs will become False, and will stay False as long as both DC inputs are True. If one DC input then becomes False the flip-flop assumes the state determined by the other input, providing it remains True at least 40 nsec.

The gating of the flip-flop inputs is external to the IC, just as with the Buffer and Inverter IC's. The output pull-up resistor is also external to the IC. Gates are normally placed on the same module as the flip-flop IC and are not available at one of the 52 connector pins since the wiring from the gate output to the flip-flop input is via etch. On many modules the AC Reset Input is wired True by connecting the AC Reset input through a resistor to +8 VDC. This eliminates external wiring to the AC Reset Input in many applications. It is possible to wire the SDS 307 in this fashion since the AC Set Input always overrides the AC Reset Input if both inputs are simultaneously True.

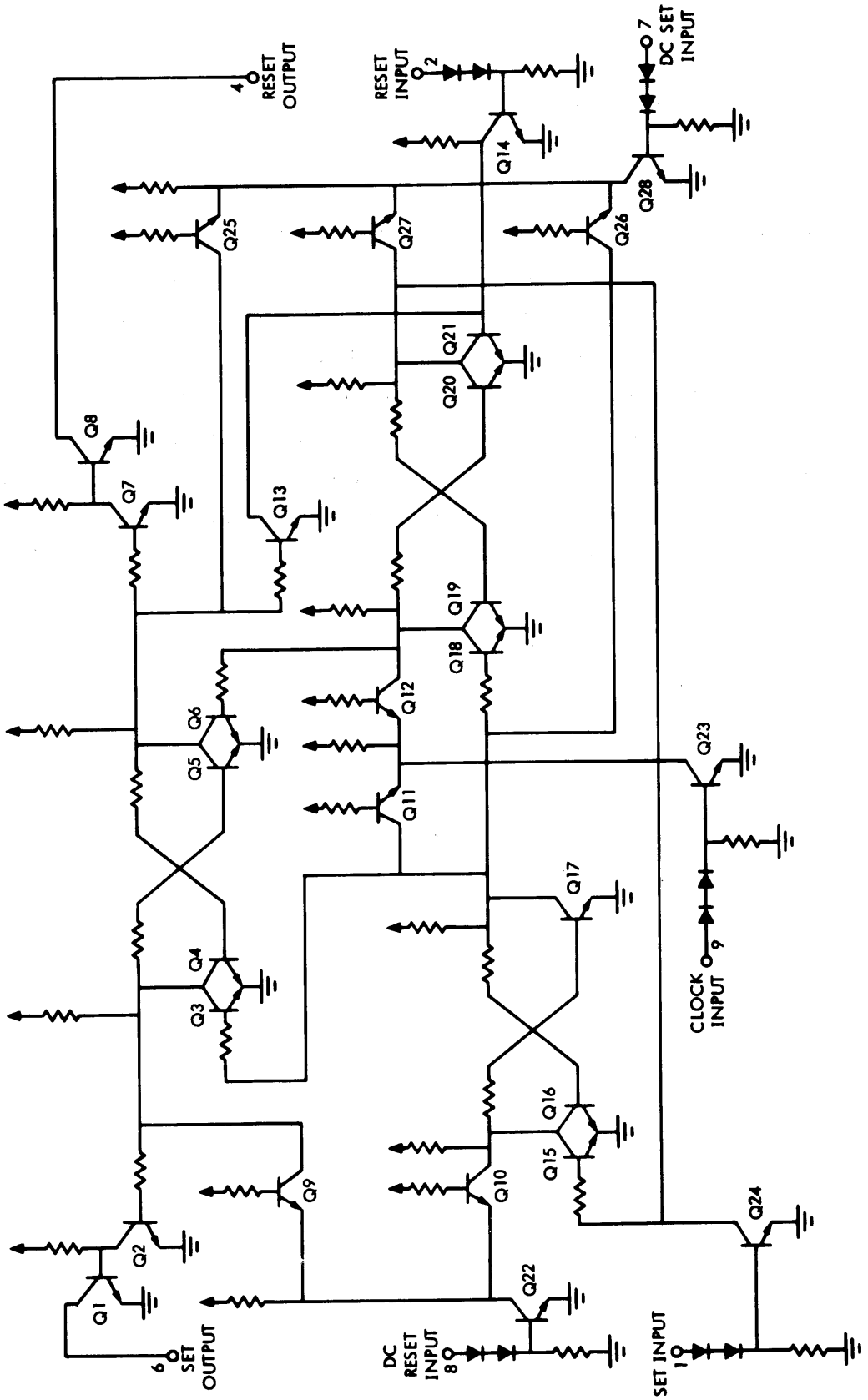
The Set Override mechanism and the other SDS 307 features can be understood by an inspection of the logic diagram. The flip-flop is a dual-rank configuration of NOR elements. The second rank (Q3, Q4, Q5, and Q6) is a simple NOR flip-flop, coupled to the output pins through buffers that each provide 60 ma (16 unit loads), normally connected to external pull-up resistors.

The first rank (Q15 through Q21) consists of two flip-flops, one for Set (Q18-Q21), and one for Reset (Q15-Q17). The two internal lines which couple the first rank to the second rank also connect to the Clock Input logic. When the Clock goes True, these two lines are clamped to ground, isolating the first rank from the second rank, so that the second rank holds its original state. During this time, while Clock is True, the Set and Reset flip-flops are primed to the states of the AC Set and Reset Inputs. When the Clock Input goes False (Trailing Edge) they assume the new states and regain control of the second rank flip-flop. Note that the outputs change to the new state on the Clock Trailing Edge. AC Inputs must be steady for 30 nsec before the Clock falls, and for 5 nsec after the Clock falls to permit the first rank flip-flops to stabilize.

The Set Inverter (Q24) always overrides inputs to the Reset Inverter (Q14) when the AC Set Input is True because it is coupled to an output of the Set flip-flop, forming a wired AND, while the Reset Inverter is coupled to an input of the Set flip-flop. This is the basis for the Set Override feature.

The second rank output is fed back to the first rank so that outputs remain unchanged when clock pulses occur and both AC inputs are False.

Note that the DC Set (MARK) and DC Reset (ERASE) inputs essentially bypass the first rank, activating the second rank directly, thus overriding the entire AC Set-Reset structure.

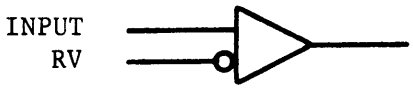


SDS307 Flip-Flop Schematic Diagram

SDS 308 DISCRIMINATOR

The SDS 308 comprises 2 microcircuit discriminators housed in a 10-lead TO-5 can. The circuit is fabricated as a semiconductor monolithic integrated circuit. It forms an integral part of Cable Receiver modules (AT10, AT11). Each discriminator circuit produces a logical "1" (+4 VDC) at the output if the input signal is greater than the Reference Voltage. On the AT10 and AT11 modules, the Reference Voltage (RV) is fixed at approx. +0.54 VDC. If the input is less than the RV, or is open (floating) the output will be a logical "0" (0 VDC).

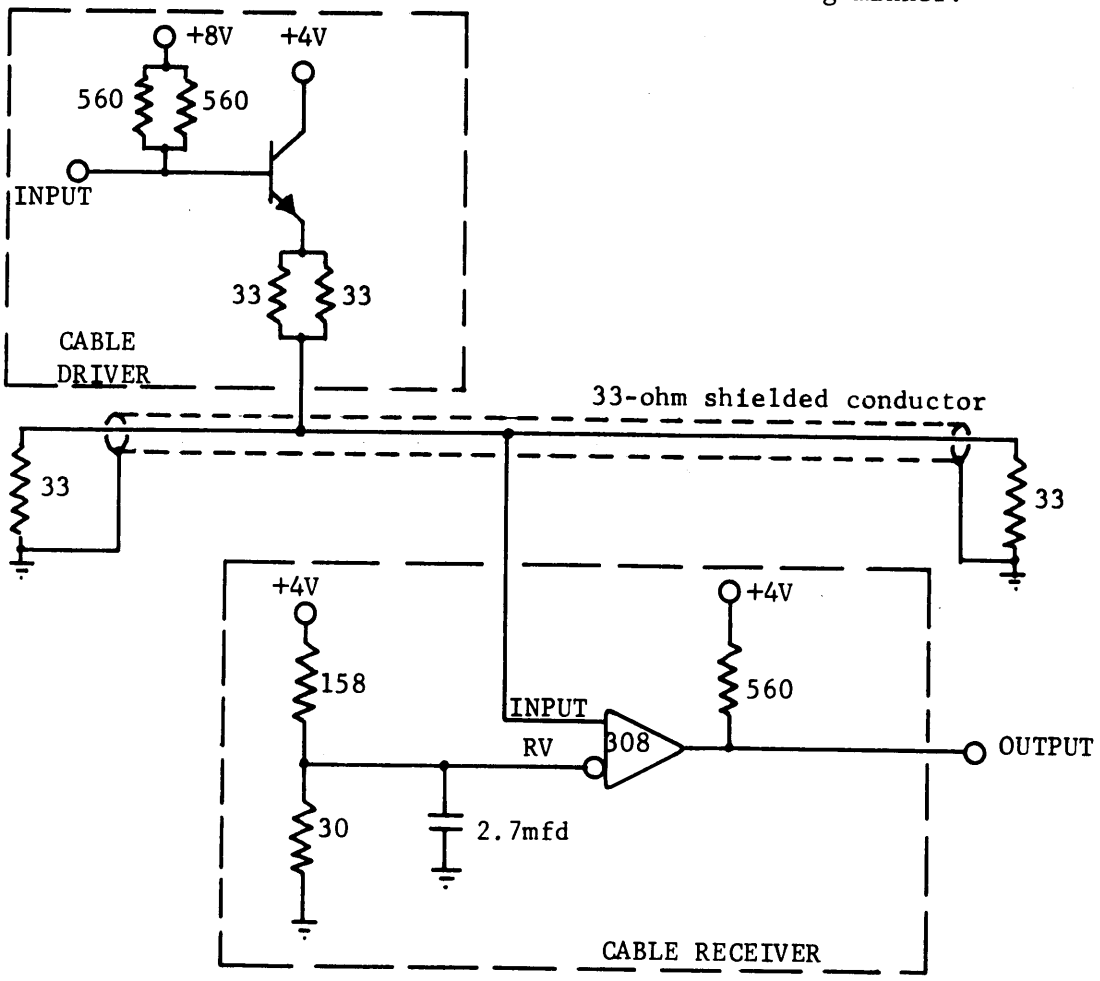
LOGIC SYMBOL (1 of 2)



INPUT	OUTPUT
> RV	+4 VDC
≤ RV	0 VDC
OPEN	0 VDC

APPLICATION

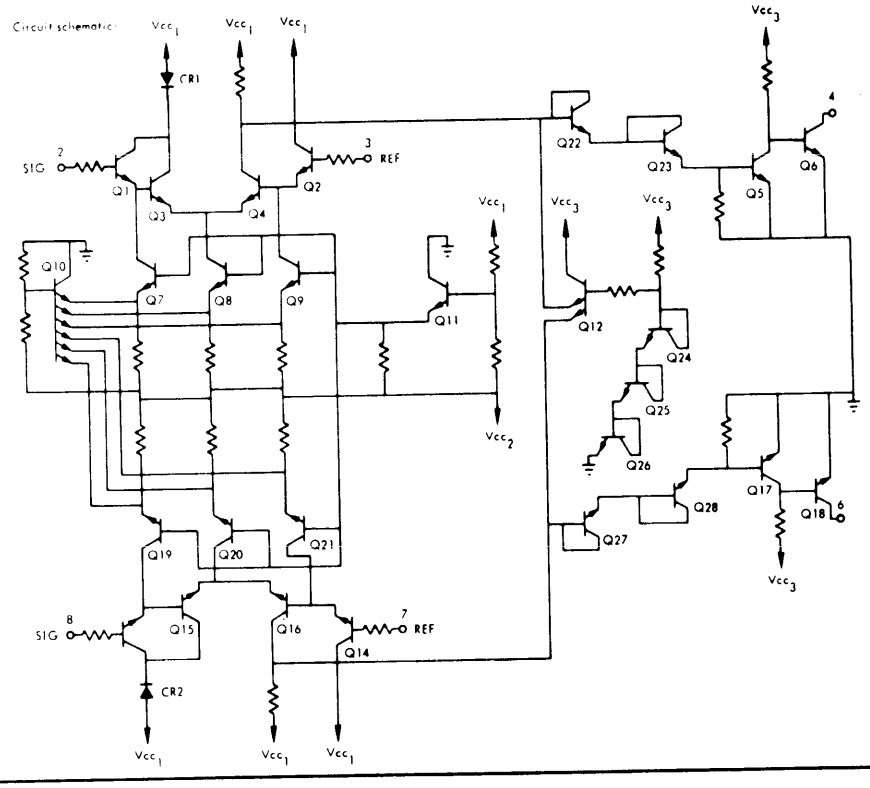
As stated before, the SDS 308 was designed primarilly to be used as part of Cable Receiver circuits, and are part of the AT10 and AT11 Cable Receiver modules. In this application, the input signal to the SDS 308 comes from a cable connector, 33-ohm cable, and a Cable Driver module in the following manner:



The input to the SDS 308 represents a high impedance to the line, causing a load of approx. 50 microamps to be absorbed. One Cable Driver can drive up to 25 Cable Receivers, however, the limit of 200 feet lengths for the 33-ohm cable normally is reached before this number of Cable Receivers can be connected to the cable.

The Cable Driver output is +2 VDC (logical "1") and 0 VDC (logical "0"). When more than 1 Cable Driver is connected to a line, the voltage on the line raises exponentially due to the decrease in emitter-follower series resistance versus the 33-ohm termination loads; this does not affect the Cable Receiver(s) performance, however, if this line is driving other, non-standard, logic, the rising line potential may be intolerable. The maximum line potential would be the collector potential of the Cable Driver emitter-follower (+4 VDC).

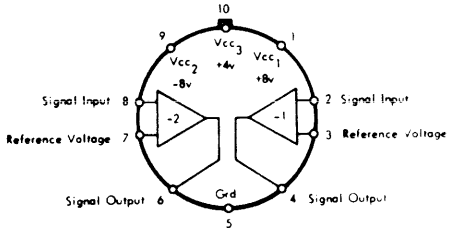
SDS 308 Discriminator Microcircuit



IC Specifications:

Housing:	Two circuits per TO-5 can
Turn-on delay:	40 nsec. max. (50% points)
Turn-off delay:	40 nsec. max. (50% points)
Typical operation:	25 nanoseconds
Output:	Same characteristics as SDS 306 buffer

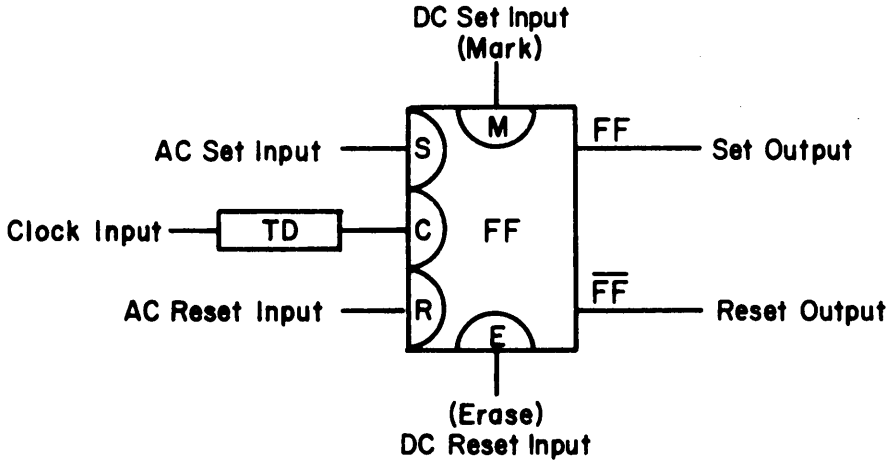
TO-5 can connections:

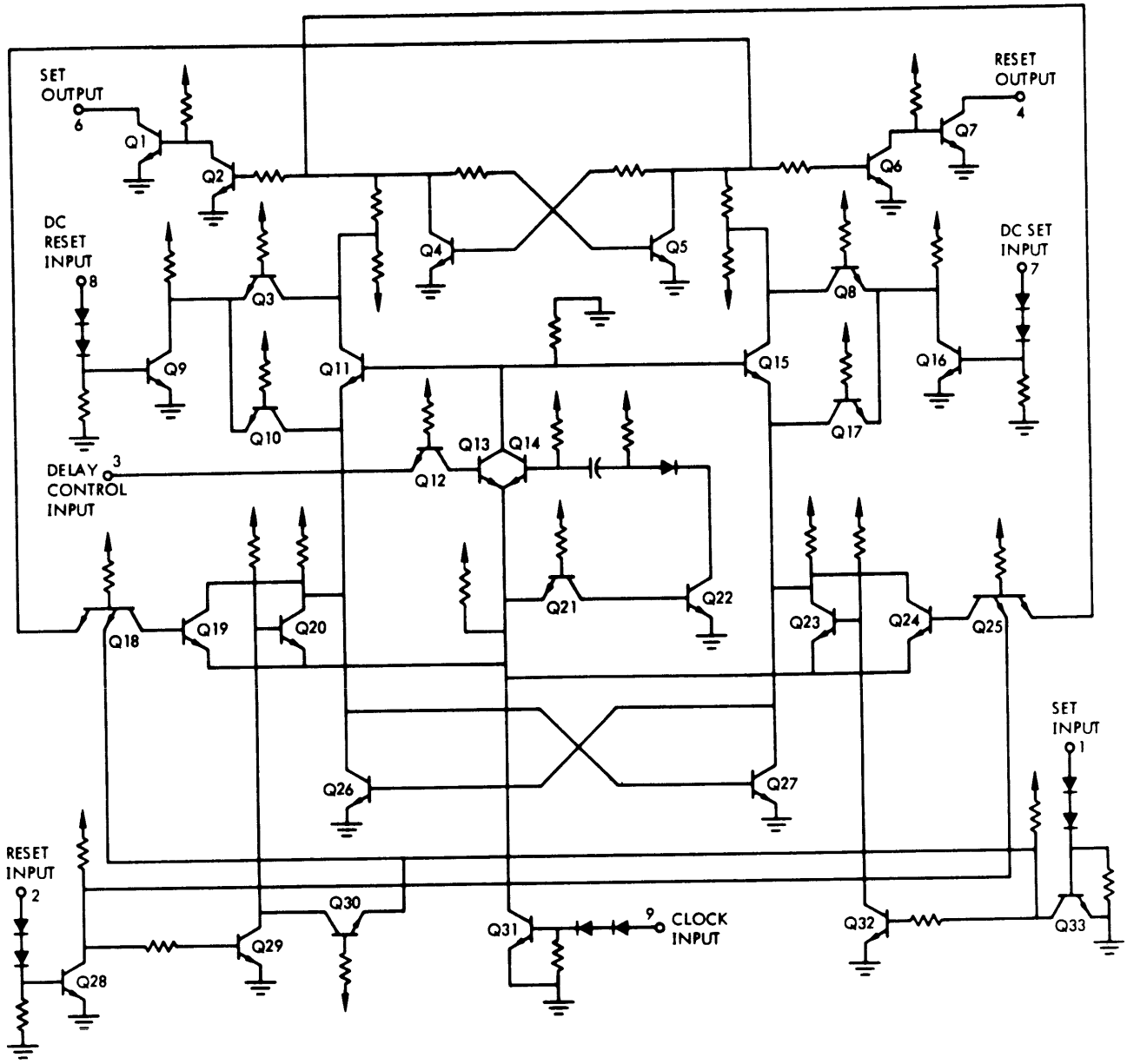


SDS 311 FLIP-FLOP

The SDS 311 is basically the same as the SDS 307, with the exception of the Delay Control Input, which is connected to pin 3 of the TO-5 can. This input provides a delayed Set and Reset Output of 80 to 200 nsec, after the fall of the Clock Input. This feature is only functional if the Delay Control Input (pin 3) is grounded. If left ungrounded, the SDS 311 operates identically to the SDS 307. The Delay Control Input affects only the Clock Input's negative transistion. DC Set (MARK) and Reset (ERASE) inputs are unaffected. The SDS 311 is an integral part of modules FT30, FT31, and FT32, and is used for serial register operations.

LOGIC SYMBOL





SDS311 Flip-Flop Schematic Diagram

LOGIC SYMBOLOGY

SECTION IV

SIGMA LOGIC SYMBOLOGY

Recently, the company decided to use logic symbology defined by the Defense Department, MIL-STD-806B, with some minor deviations. The implementation of MIL-STD-806B logic symbology affects logic diagrams for units currently undergoing documentation, and will not be retroactive.

Prior to this recent decision, logic diagrams produced by Technical Publications as part of their Technical Manuals have been drawn to a standard called ASA Y32.16-1965 which conformed roughly to what was to have been line printer-drawn diagrams. The idea of line printer-generated diagrams was short-lived, and no effort is being made to pursue the idea. Consequently, there are manuals in existence which have logic diagrams drawn to that standard. No attempt will be made here to explain that type of logic symbology since those manuals include an adequate explanation.

When drawings first started appearing for Sigma equipment which were drawn by the designers and engineers they conformed to the standard set up by the company for the older 9-Series product line, and is generally referred to as "9-Series Logic Symbology". Training adopted this standard partly because the designers and engineers adopted it, but mainly because Training felt that the 9-Series symbology was adequate for expressing Sigma logic implementation with only a few additional symbols, and that Customer Engineers who had worked on the 9-Series equipment would find it easier to learn Sigma equipment using familiar symbology. Further, some of the peripheral devices developed for Sigma utilized some 9-Series hardware, therefore, it was thought desireable to keep the supporting documentation compatible.

It is obvious that in learning and troubleshooting Sigma equipment you are going to be faced with at least 2 different logic symbology standards, the older 9-Series Symbology and MIL-STD-806B Symbology, until revisions and updating of material causes the 9-Series Symbology to phase out.

In the following pages are representative diagrams for both 9-Series and MIL-STD-806B Symbology, presented in two separate parts with an explanation as to their use (when necessary) and conventions. These two parts of this section should be considered as a reference area when you are in doubt as to the interpretation of a logic symbol; you are not expected to study these symbols at this time and commit them to memory.

Before you look the symbols over, keep in mind that the emphasis placed on logic diagrams as a maintenance aid only survives in isolated areas within the total Sigma Product Line, usually restricted to certain peripheral devices where the number of logic structures is small.

Logic diagrams, because they carry a strong visual impact, are drawn primarily for use in training, whether they appear in Technical Manuals or in Training Documents, and it is for this use, while you are learning the equipment, that familiarity with logic symbols really is important.

9-Series Symbology

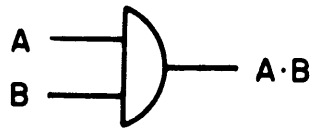
In applying 9-Series Symbology to Sigma circuit elements, many of the conventions have been retained as to the symbol shapes. Since the Sigma modules do have circuits not found in the 9-Series equipment, some new symbols have been added.

Each of the symbols is defined by a Boolean truth table when applicable. Sigma uses "positive logic", which means that a logic "1" equals a relatively high level (+4VDC, unless otherwise noted), and a logic "0" equals a relatively low level (0 VDC).

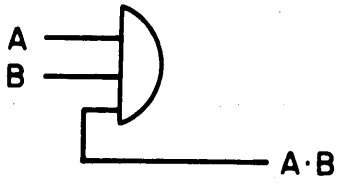
9-Series Symbology is based on a relationship between symbol shape and the type of hardware curcuitry it is trying to represent. This characteristic will be important when you are trying to see the differences between the 9-Series Symbology and MIL-STD-806B Symbology.

AND GATE

(no isolation diode)



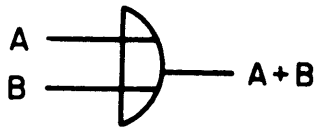
(with isolation diode)



A	B	OUTPUT
0	0	0
0	1	0
1	0	0
1	1	1

note: an open input has same effect as +4VDC

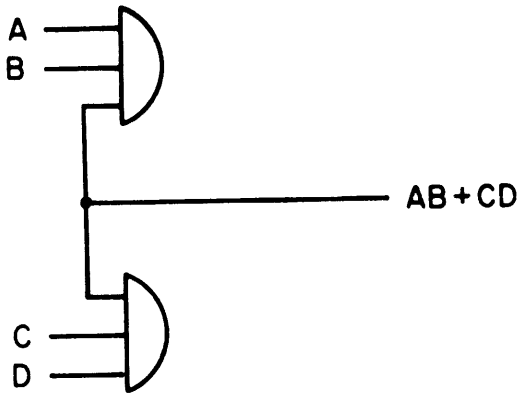
INCLUSIVE OR GATE



A	B	OUTPUT
0	0	0
0	1	1
1	0	1
1	1	1

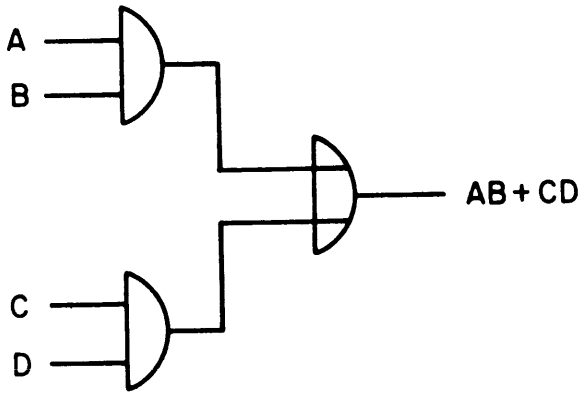
note: an open input has same effect as +4VDC

AND/OR COMBINATION

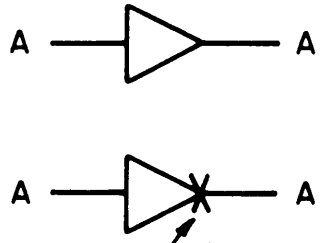


A	B	C	D	OUTPUT
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

(identical circuits)

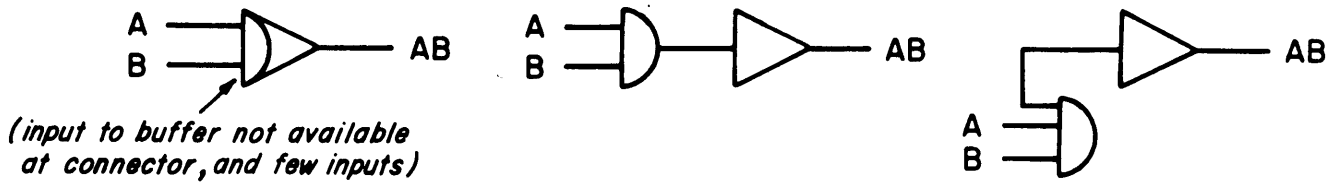


BUFFER

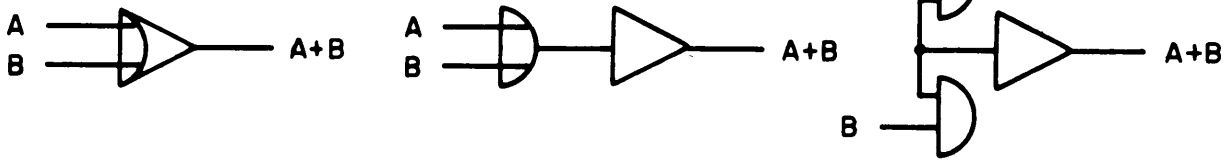


INPUT	OUTPUT
0	0
1	1
OPEN	1

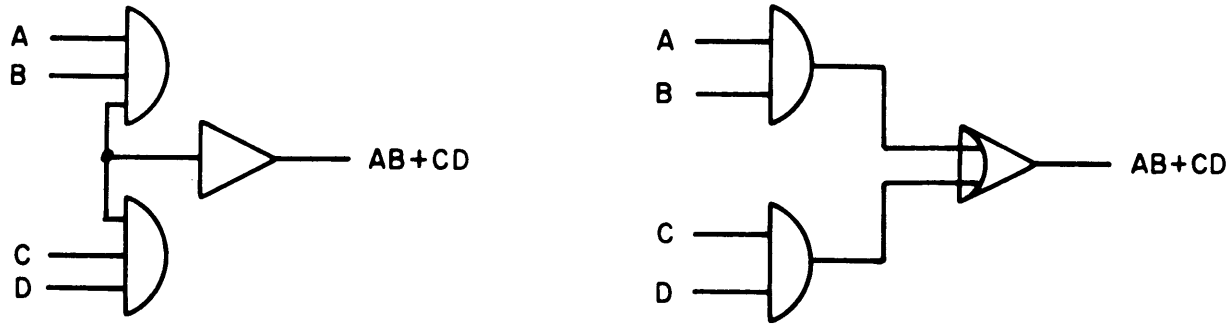
BAND



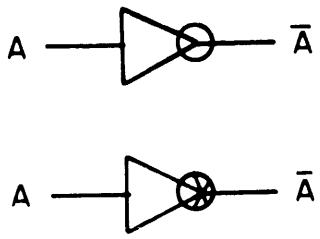
BOR



BAND/BOR

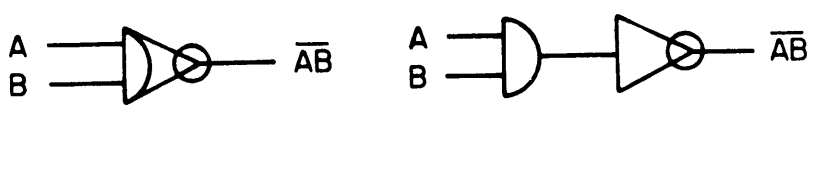


INVERTER

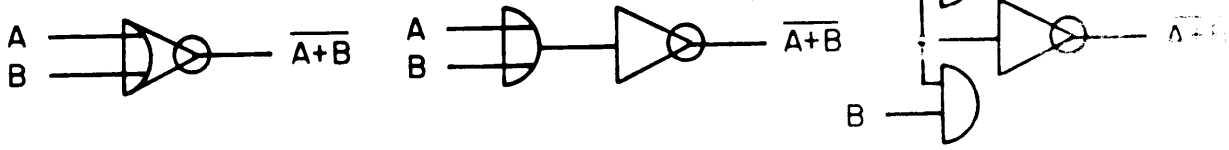


INPUT	OUTPUT
0	1
1	0
OPEN	0

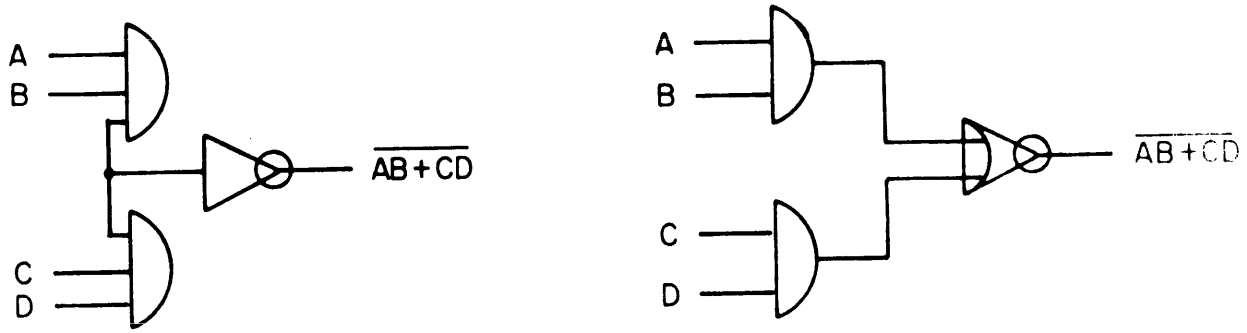
NAND



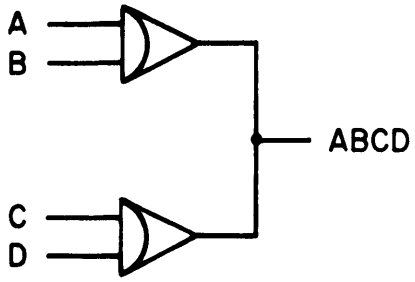
NOR

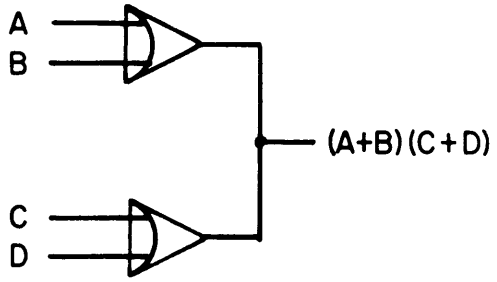


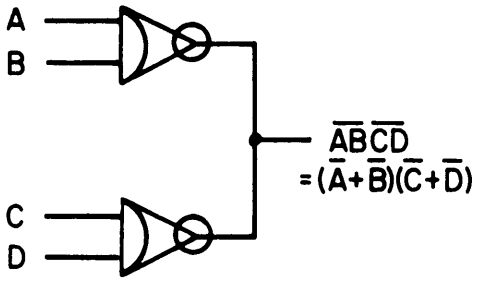
NAND/NOR

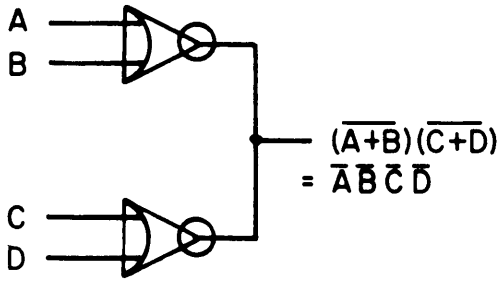


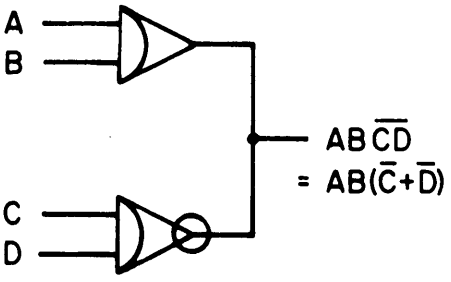
WIRED OUTPUT — EXAMPLES

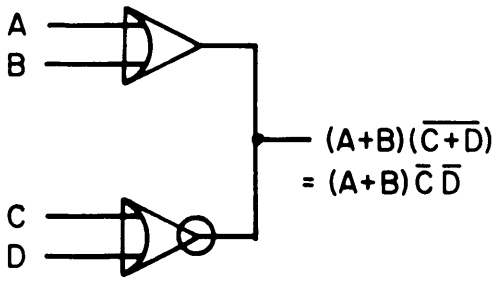












Note: If one element has a OVDC output (output transistor conducting), then the output line is clamped at OVDC.

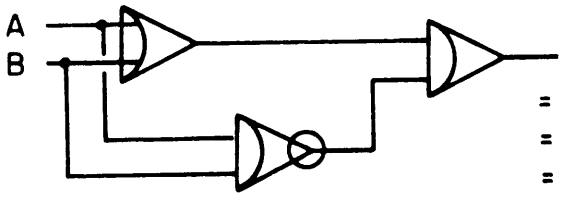
CLOCK DRIVER

INPUT	OUTPUT
0V	0V
+4V	+4V
OPEN	+4V

EXCLUSIVE OR GATE

2-INPUT

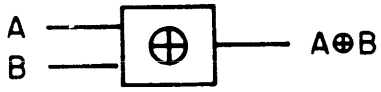
(Implicit)



$(A+B)\,\overline{AB}$
$= (A+B)(\bar{A}+\bar{B})$
$= A\bar{B} + \bar{A}B$
$= A \oplus B$

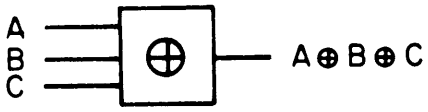
A	B	OUTPUT
0	0	0
0	1	1
1	0	1
1	1	0

(Explicit)



$A \oplus B$

3-INPUT

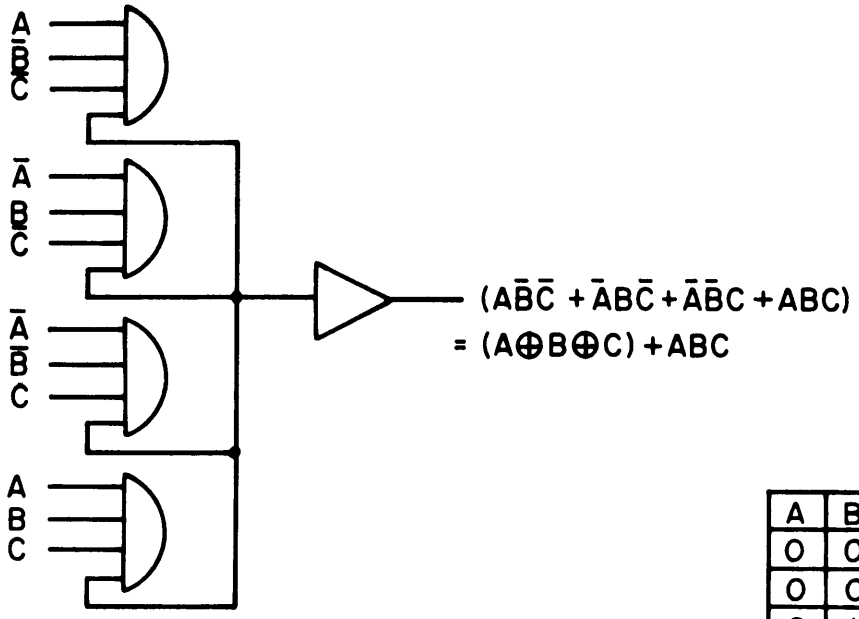


$A \oplus B \oplus C$

A	B	C	OUTPUT
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

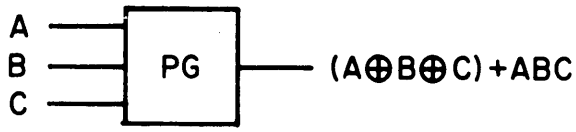
PARITY GENERATOR

(Implicit)



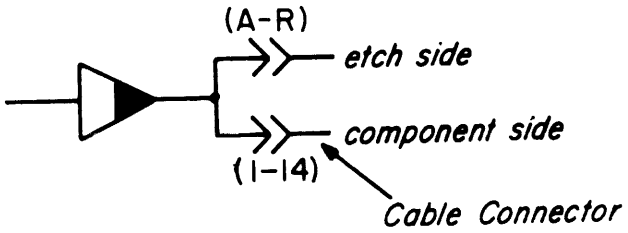
A	B	C	OUTPUT
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

(Explicit)



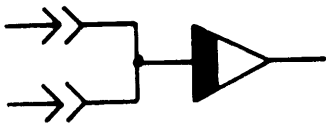
Note: the Parity Generator has a true output when an odd number of trues are present at the inputs.

CABLE DRIVER



INPUT	OUTPUT
+4V	+2V
0V	OPEN
OPEN	+2V

CABLE RECEIVER



INPUT	OUTPUT
0V	0V
+2V	+4V
OPEN	0V

* Input threshold is +0.54VDC

8-VOLT INTERFACE DRIVER

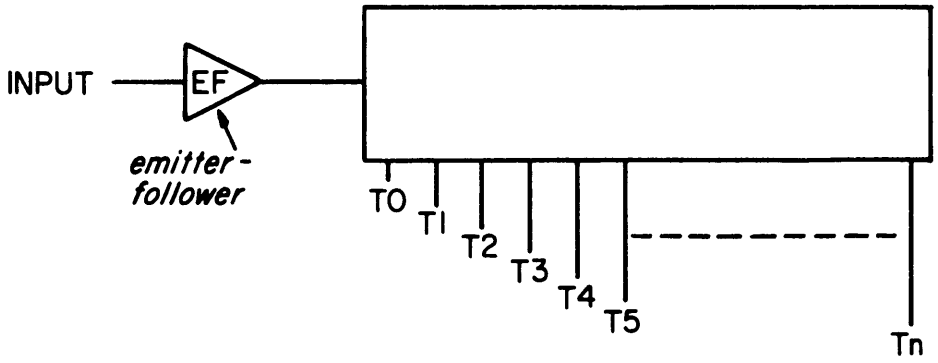
INPUT	OUTPUT
0V	+8V
+4V	0V
OPEN	+8V

8-VOLT INTERFACE RECEIVER

INPUT	OUTPUT
0V	+4V
+8V	0V
OPEN	0V

* Input threshold is +4VDC

MULTI-TAP DELAY LINE



INPUT	OUTPUT
0V	-4V
+4V	+4V
OPEN	-4V

(delayed)

The Multi-Tap Delay Lines are tapped at fixed increments for their entire length, the increment being 20 nsec for the 600 nsec DT11 module, and 10 nsec for the 300 nsec DT14 module. The voltage levels at the delay line taps are nominally +4 VDC (Logic "1"), and -4 VDC (Logic "0"). Consequently, they require special sensor circuits to operate from the taps which have a high impedance input, to avoid loading down the delay line. Several sensor circuits may be connected to a tap, however, the interconnecting wire should be as short as possible to minimize the capacitive load on the delay line.

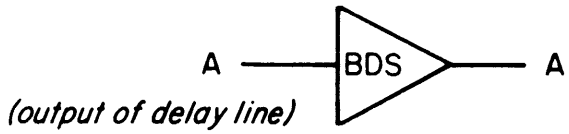
The Emitter-follower circuit at the input accepts 0 VDC to +4 VDC excursions and drives the delay line with +4 VDC to -4 VDC excursions. The Emitter-follower is normally gated by an AND/OR COMBINATION input gate.

DELAY ELEMENT

INPUT	OUTPUT
0V	0V
+4V	+4V
OPEN	0V

(delayed)

BUFFER DELAY LINE SENSOR

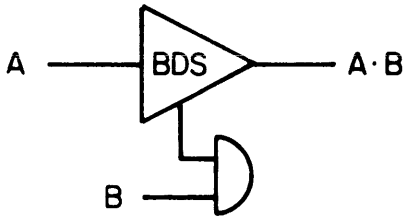


INPUT	OUTPUT
-4V	0V
+4V	+4V
OPEN	+4V

*

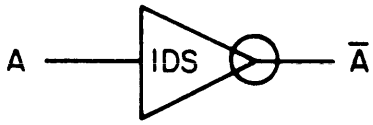
* *Input threshold is 0VDC*

GATED BUFFER DELAY LINE SENSOR



A	B	OUTPUT
-4	0V	0V
-4	+4	0V
+4	0V	0V
+4	+4	+4V

INVERTER DELAY LINE SENSOR



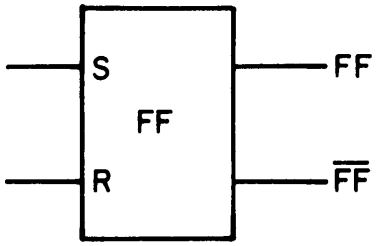
INPUT	OUTPUT
-4V	+4V
+4V	0V
OPEN	0V

*

* *Input threshold is 0VDC*

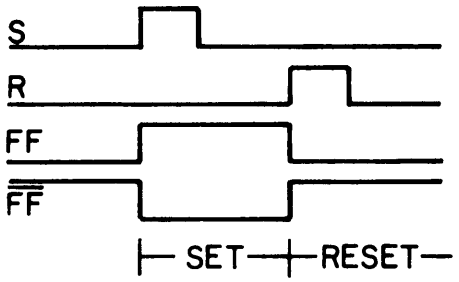
Note: IDS circuits are not gated.

DC FLIP-FLOPS

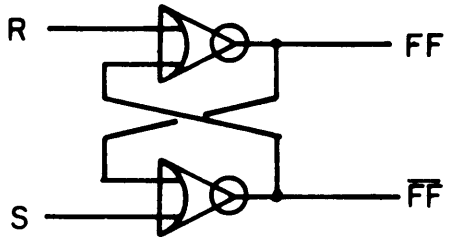


S = DC Set Input
R = DC Reset Input
FF = Set Output
$\overline{FF}$ = Reset Output

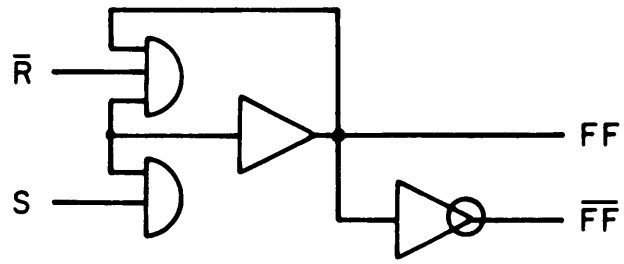
Timing

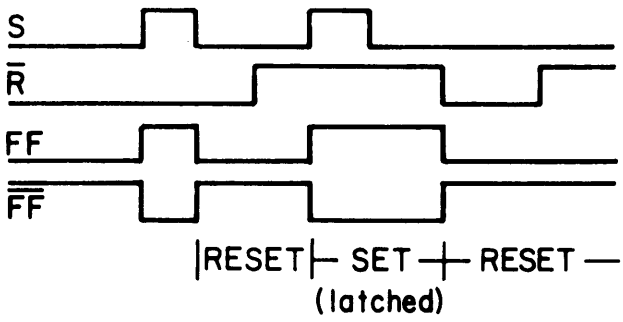


Typical implementation



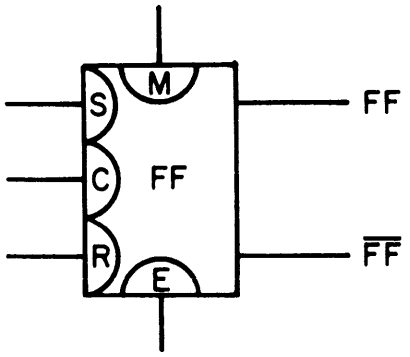
DC Flip-Flops may also be implemented and shown as BUFFER LATCH circuits:





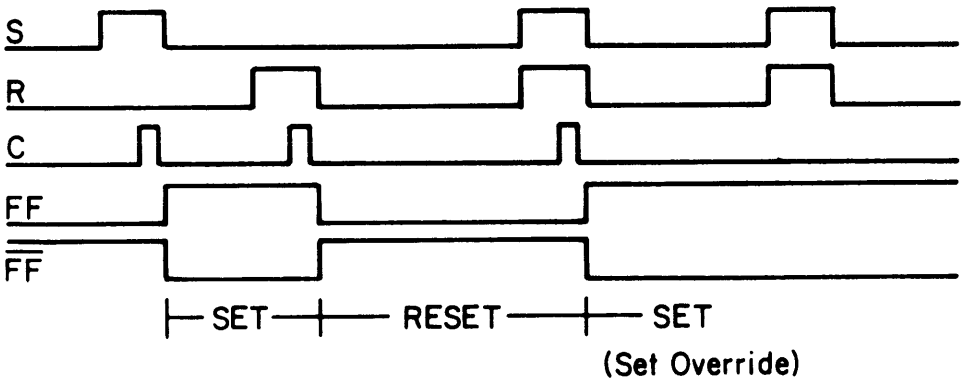
S = Set Input
$\overline{R}$ = Latch Control
FF = Set Output
$\overline{FF}$ = Reset Output

AC FLIP-FLOP (using SDS 307 or 311 IC)



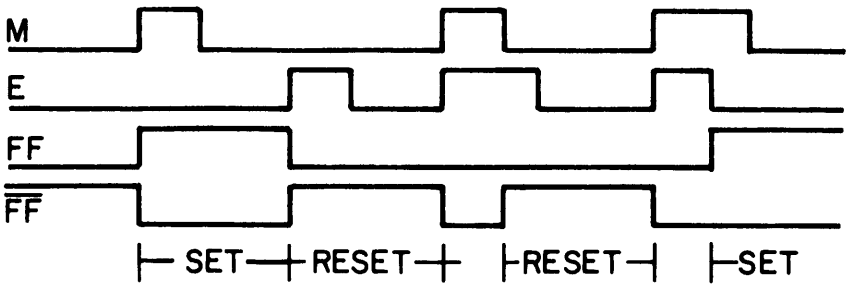
S = AC Set Input
C = AC Clock Input
R = AC Reset Input
M = DC Set Input – MARK (FORCE)
E = DC Reset Input – ERASE
FF = Set Output
$\overline{FF}$ = Reset Output

AC MODE TIMING



Note: An open input is a True input.

DC MODE TIMING



OTHER SYMBOLS

The symbology for other (specialized) logic or non-logic functions are usually as a rectangle with an associative mnemonic (name) within the rectangle:

MIL-STD-806B Symbology

MIL-STD-806B logic symbology is an attempt to standardize all logic diagrams used by the Defense Department. Their reasons for creating such a standard is obvious, since they purchase equipment from many different manufacturers.

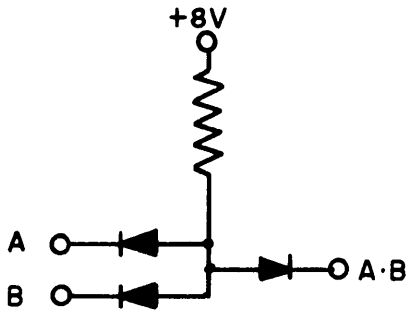
This standard is essentially hardware-independent and function-oriented. This means that the symbology attempts to represent Boolean functions rather than trying to differentiate between different types of circuitry, as is done in the 9-Series. No difference in symbology exists, for instance, between a passive (diode-resistor) circuit which produces an AND function, and an active circuit (diode-resistor-transistor) which also produces an AND function. The essential information is that an AND function is produced at a certain point.

MIL-STD-806B is also logic convention-independent in that the standard applies to both "positive" and "negative" logic conventions. SDS uses the positive logic convention as mentioned earlier.

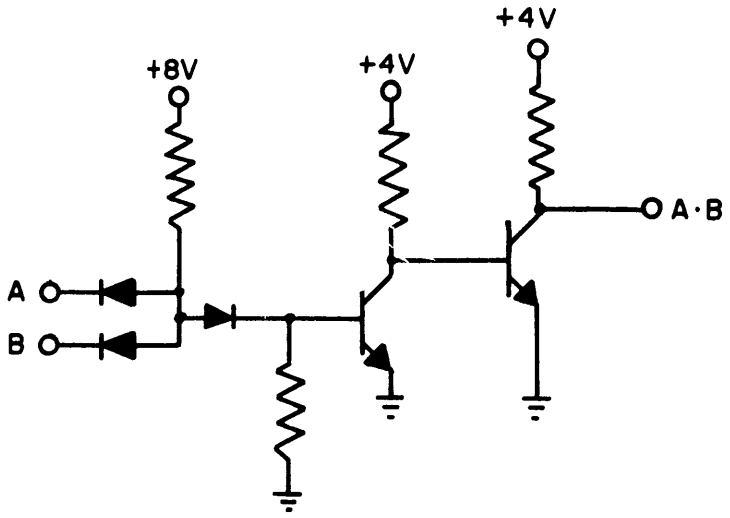
The symbols available in MIL-STD-806B are capable of representing the bulk of logic functions found in most digital systems, however, most companies have found a need to modify or add some symbols to represent proprietary logic functions.

Hardware-Indiependence

There are many ways to implement any given Boolean function. A simple AND gate could be implemented using either just diode-resistor logic, or diode-resistor gating feeding transistor circuitry for buffering and current gain. The resultant Boolean function is the same in both cases. Thus:

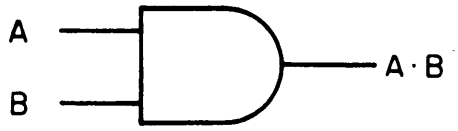


CIRCUIT 1

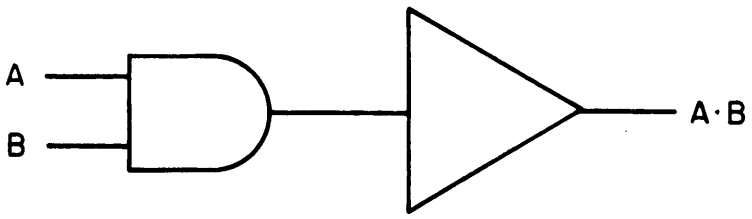


CIRCUIT 2

are both AND gates, capable of being represented by the same logic symbol:



unless, in circuit #2, the transistor logic section was located on a different module or on the same module with unique pin numbers. In this case the logic symbology could be shown as:



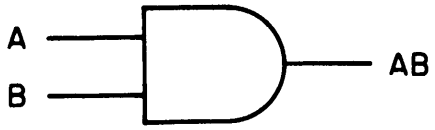
so that module and pin information could be called out in detailled logic diagrams.

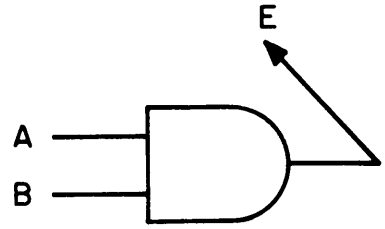
The basic assumption in representing functions rather than circuitry is that in troubleshooting it is more important to understand and verify the relationship between input and output signal(s) than to know what kind of circuitry is involved.

This assumption is argumentative in that active elements (transistor logic) insert stage delays (typically 18 nanoseconds in Sigma) whereas passive elements (diode-resistor logic) do not insert any significant delay. This difference could be important in high-speed logic analysis. This can be overcome, however, by representing active elements which have input gating as two separate symbols as shown above.

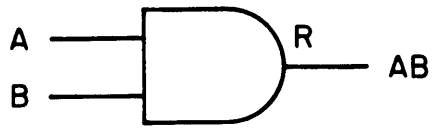
The following pages reflect the logic symbols used in MIL-STD-806B for the various Boolean functions. No attempt is made to analyze these symbols in the detail used by the actual MIL-STD-806B document. Truth tables are not shown, but can be related to those truth tables shown for the 9-Series symbols.

AND GATE

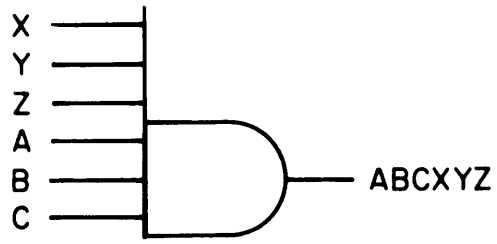


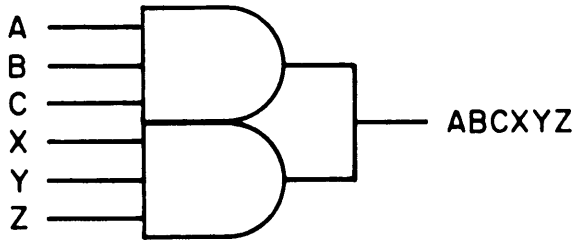


"E" means that the output of this circuit is an extension to the input of another circuit at some point other than its "normal" input.



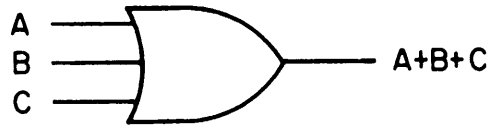
"R" means that an output resistor is not supplied as part of the etch circuitry, and must be supplied externally.

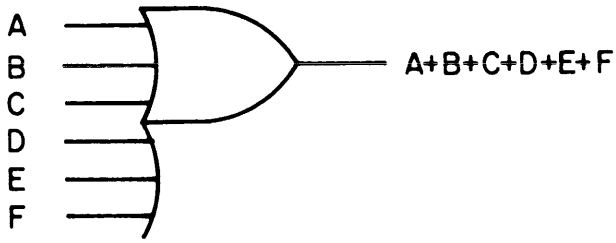




EXTENDED INPUTS

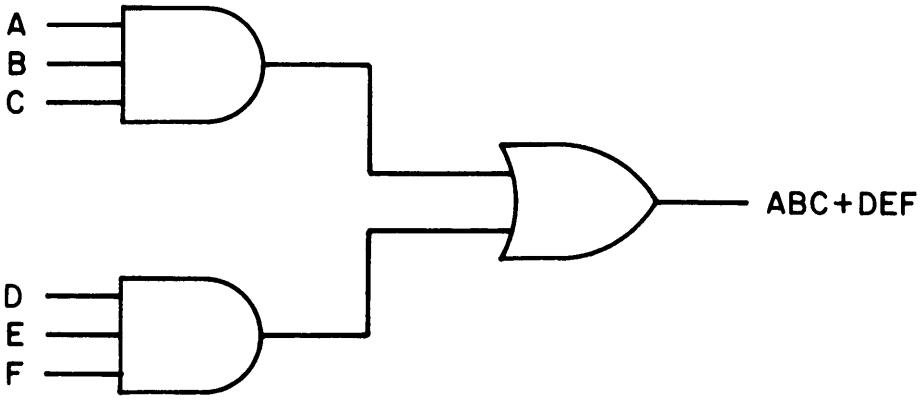
INCLUSIVE-OR GATE



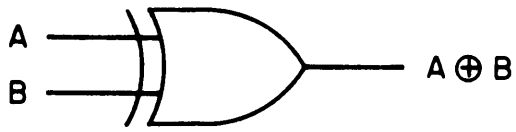


EXTENDED INPUTS

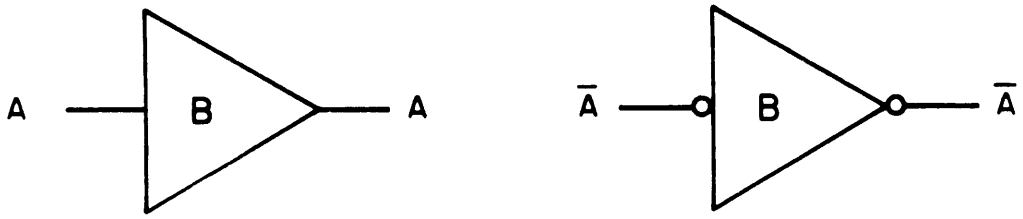
AND/OR COMBINATION



EXCLUSIVE-OR

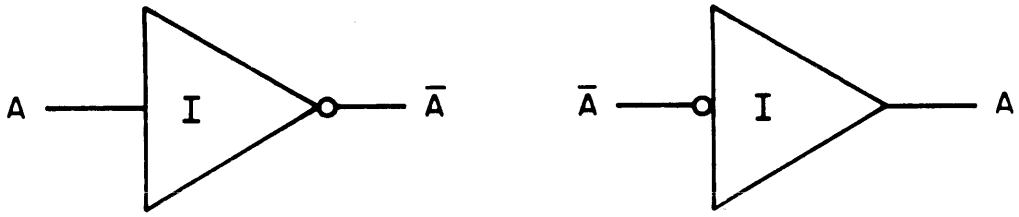


BUFFER



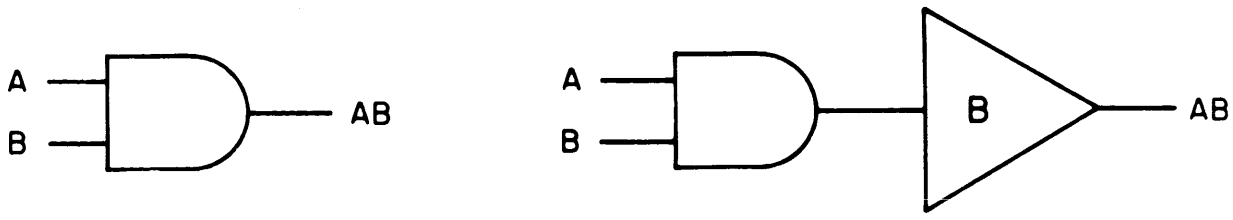
"o" symbol indicates a logic "0"(0VDC), its absence indicates a logic "1"(+4VDC)

INVERTER



BAND

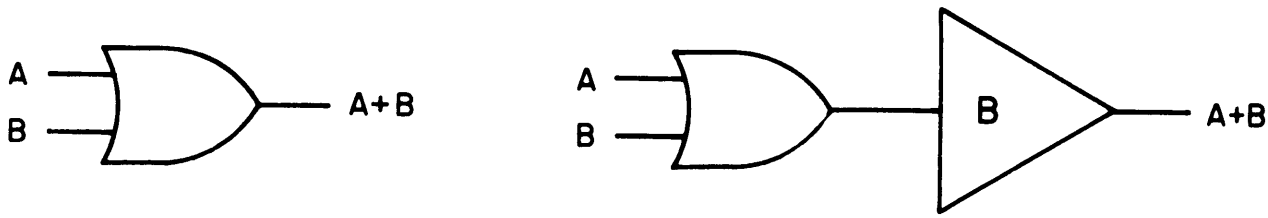
(identical circuits)



(preferred)

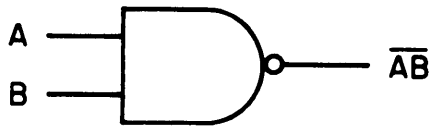
BOR

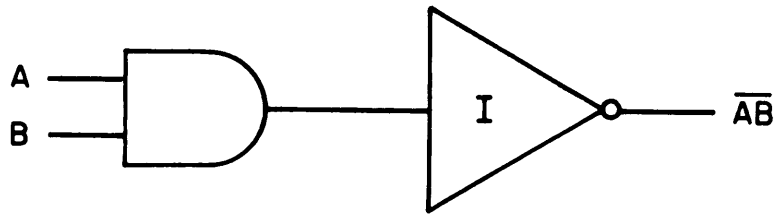
(identical circuits)



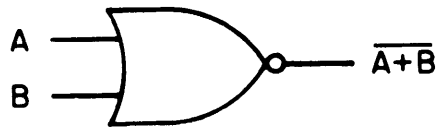
(preferred)

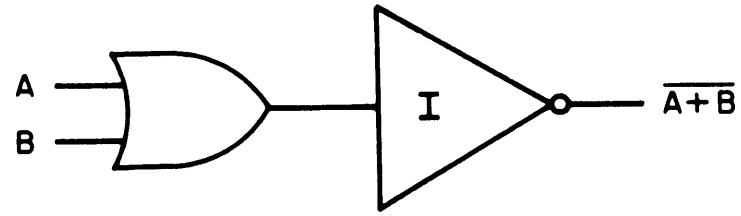
NAND



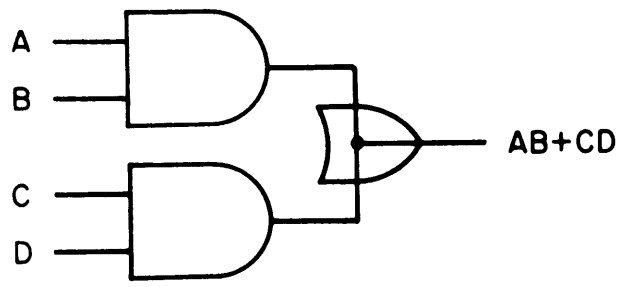


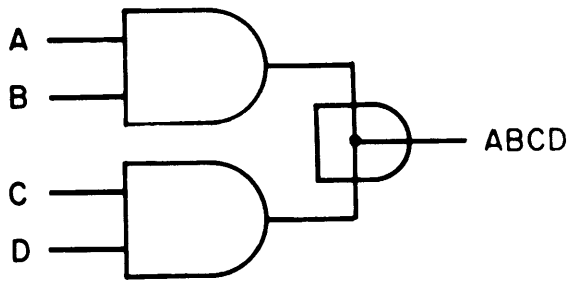
NOR

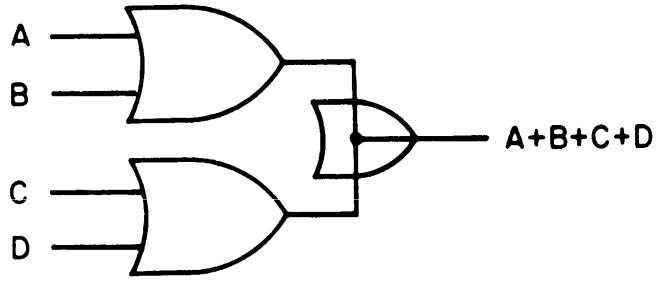


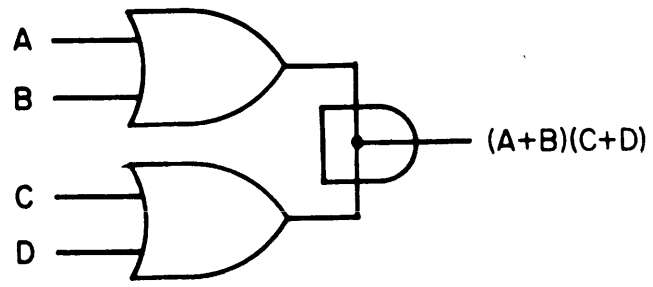


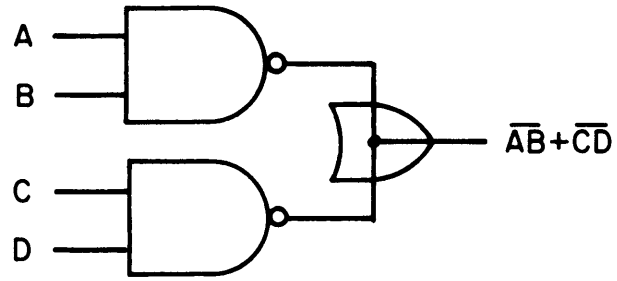
WIRED OUTPUTS

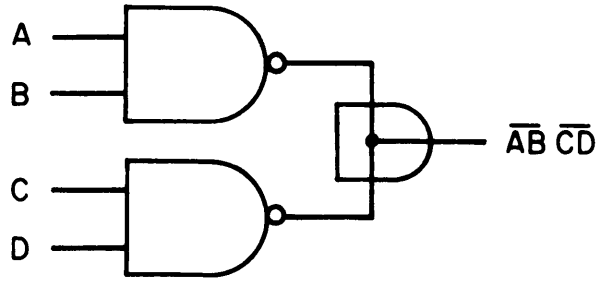


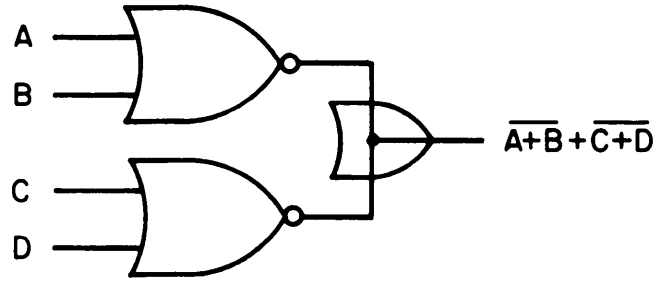


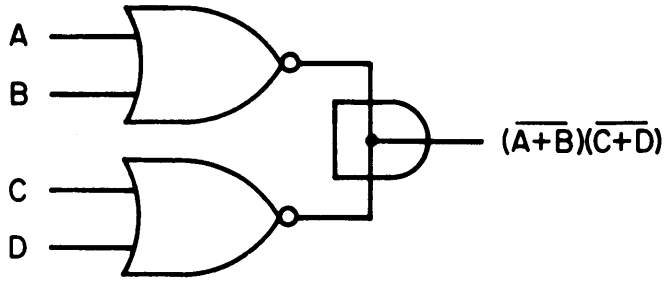


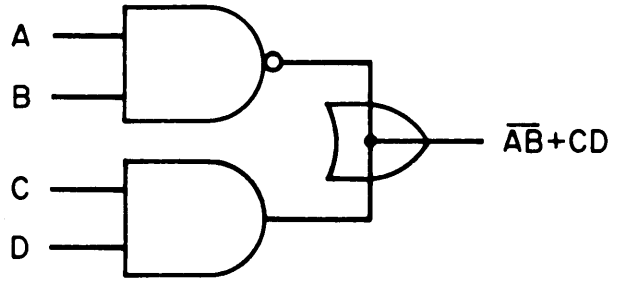


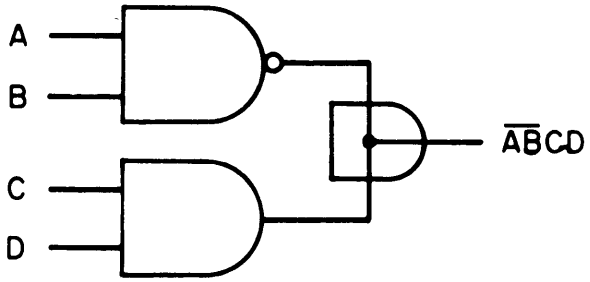

A
B
C
D
$\overline{AB}+\overline{CD}$

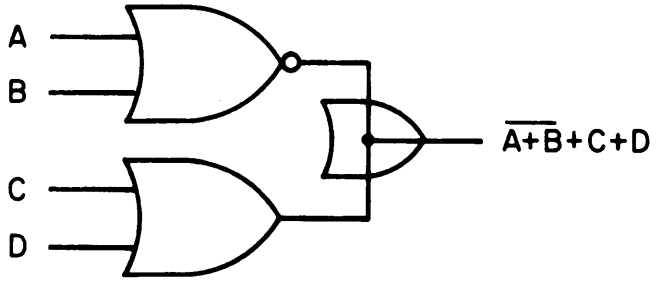

A
B
C
D
$\overline{AB}\,\overline{CD}$

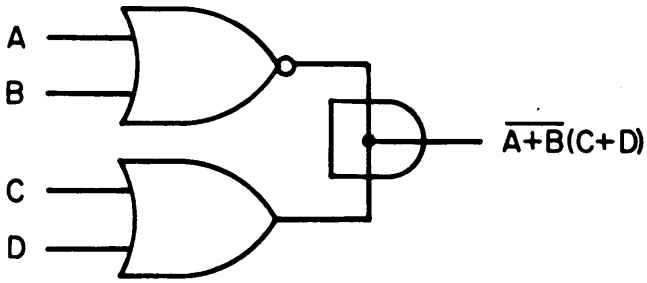

A
B
C
D
$\overline{A+B}+\overline{C+D}$


A
B
C
D
$(\overline{A+B})(\overline{C+D})$

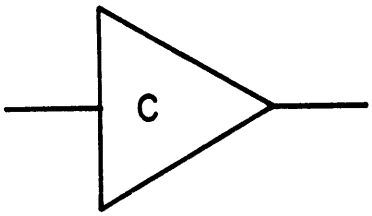

A
B
C
D
$\overline{AB}+CD$


A
B
C
D
$\overline{AB}CD$

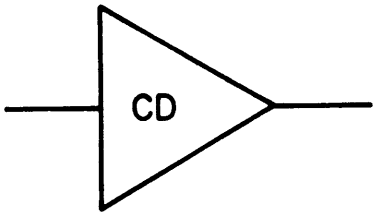

A
B
C
D
$\overline{A+B}+C+D$


A
B
C
D
$\overline{A+B}(C+D)$

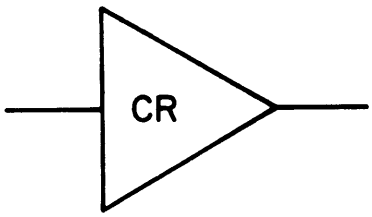
CLOCK DRIVER



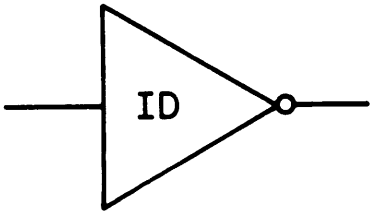
CABLE DRIVER



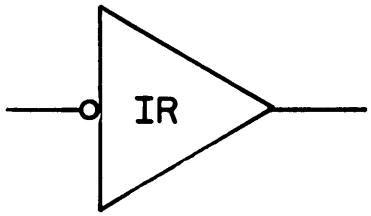
CABLE RECEIVER



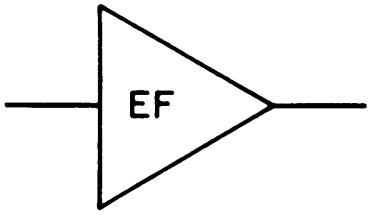
8-VOLT INTERFACE DRIVER



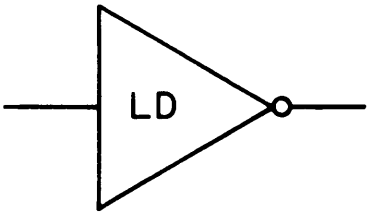
8-VOLT INTERFACE RECEIVER



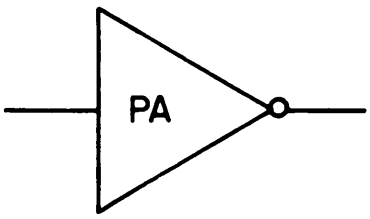
EMITTER FOLLOWER



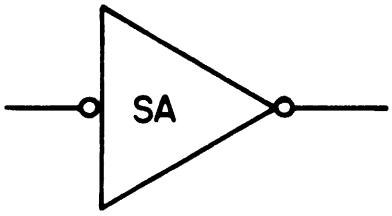
LAMP DRIVER



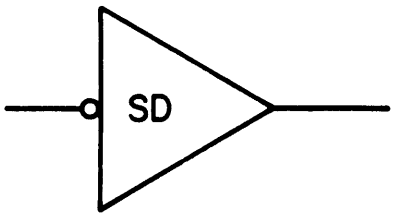
PREAMPLIFIER



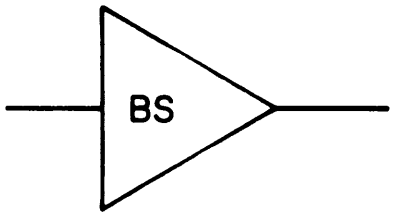
SENSE AMPLIFIER



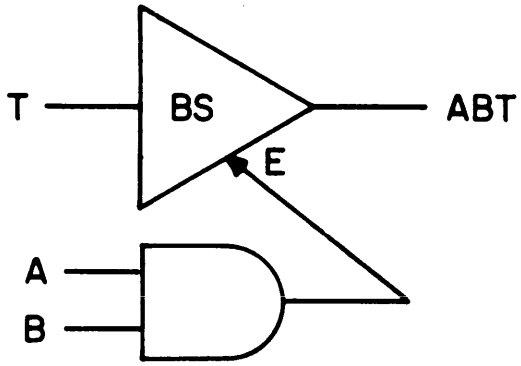
SENSE DISCRIMINATOR



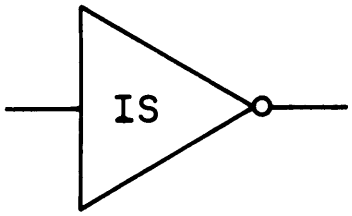
BUFFER DELAY LINE SENSOR



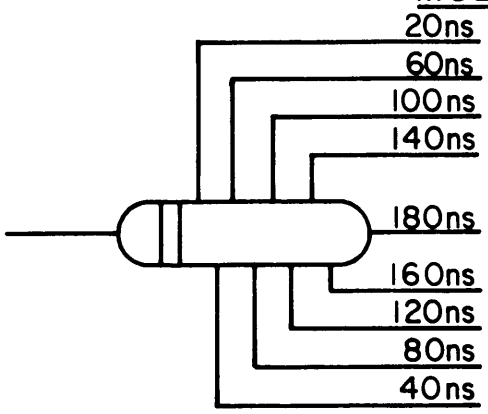
GATED BUFFER DELAY LINE SENSOR



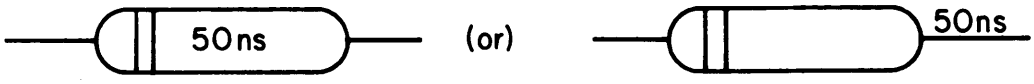
INVERTER DELAY LINE SENSOR



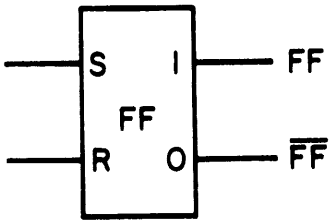
MULTI-TAP DELAY LINE



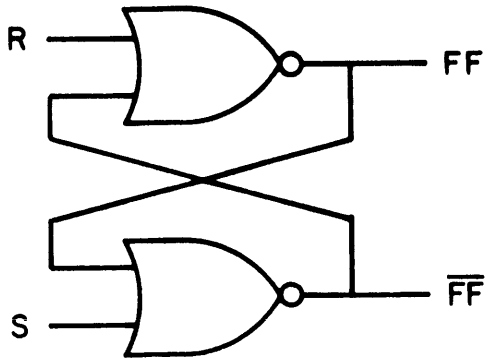
DELAY ELEMENT



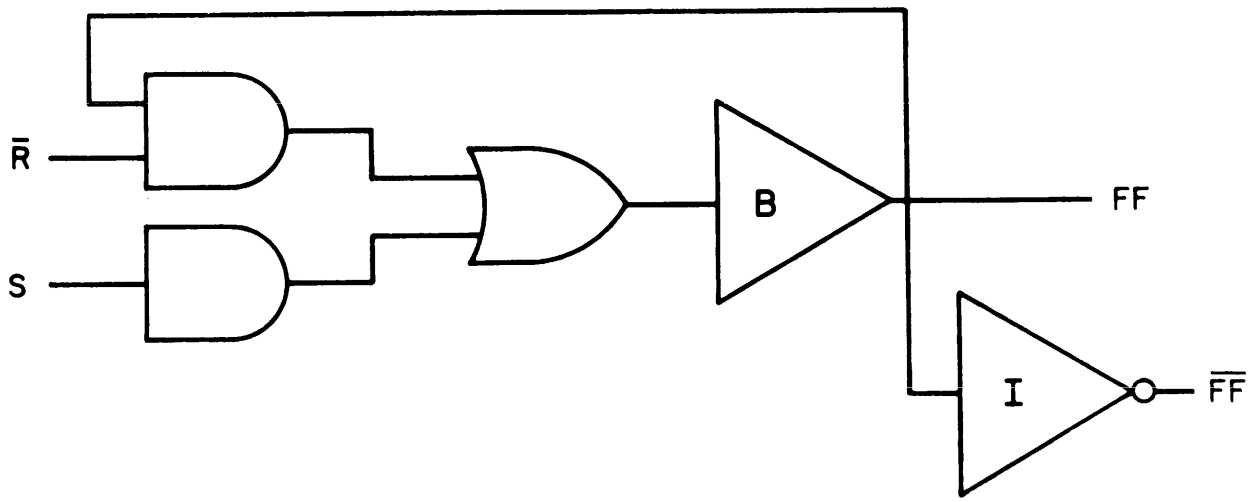
DC FLIP-FLOPS



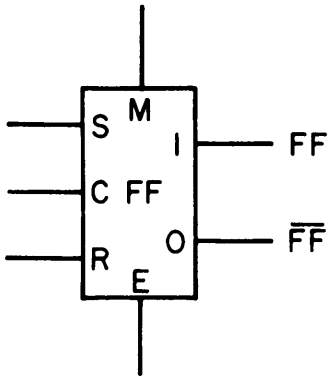
(OR)



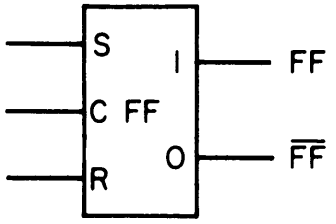
BUFFER LATCH



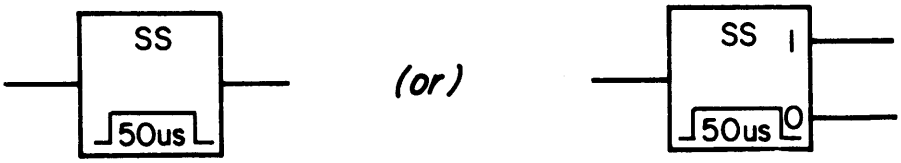
AC FLIP-FLOPS



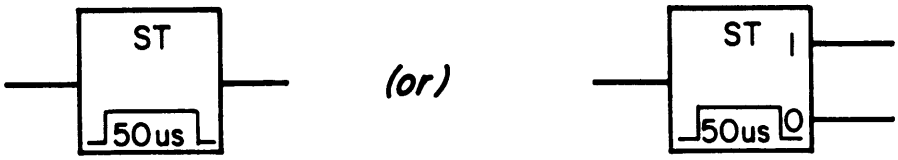
(or)



SINGLE-SHOT



SCHMITT TRIGGER



OTHER SYMBOLS

LOGIC IMPLEMENTATION

SECTION V

Through the Automated Logic System, used in the Sigma product development, SDS shifted the emphasis away from logic diagrams as a source for troubleshooting documentation and concentrated rather on the use of logic equations.

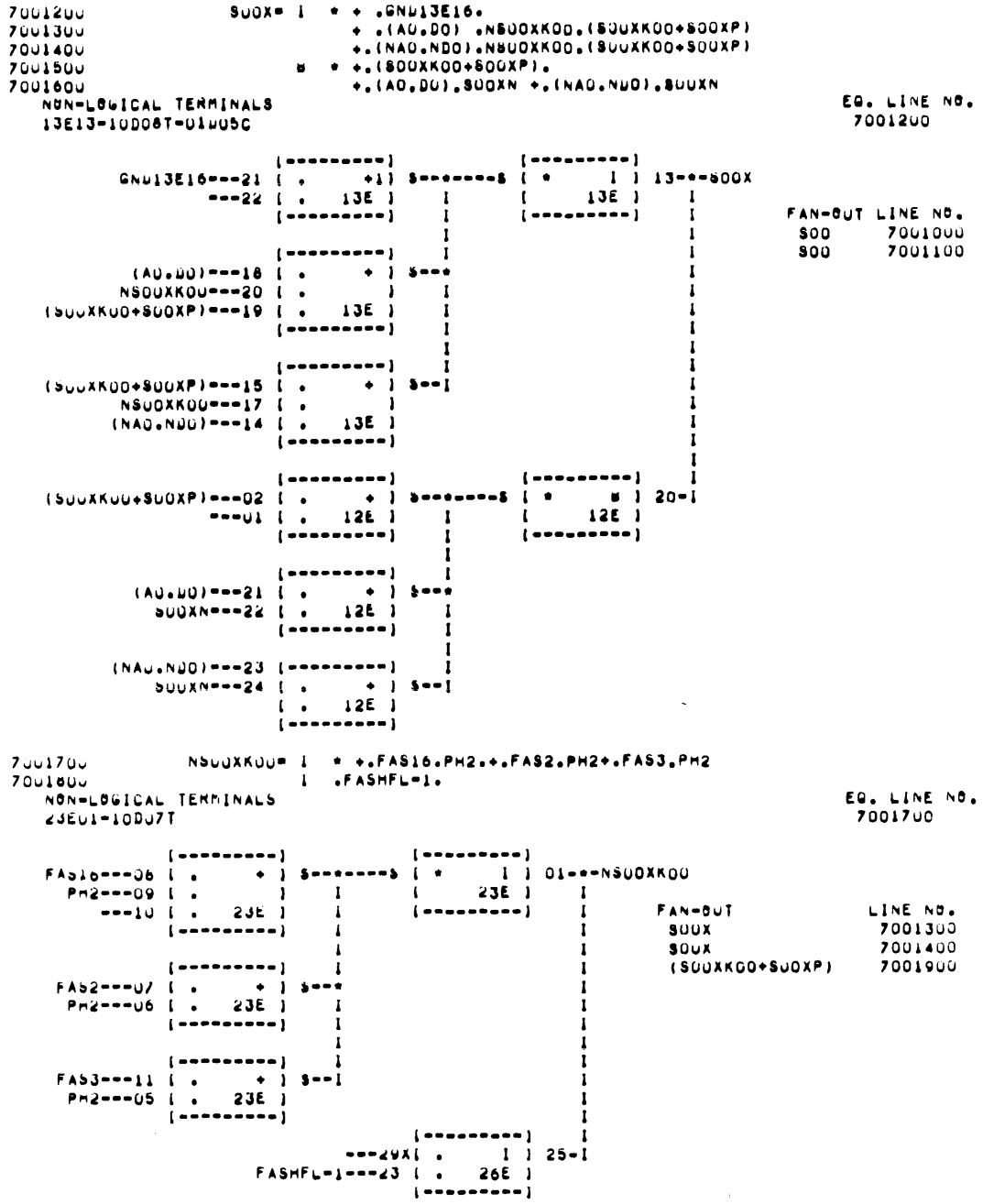
Using logic equations in lieu of diagrams is not a new idea in the industry. Other companies have been operating under this concept for years

One of the plans for the Automated Logic System was to produce automated logic diagrams from the same program (LOTRAN) that produced the equations. The idea was to use the automated (implemented) equations as an input to a routine which would convert the equation format into a diagram format suitable for line printer output. The diagrams would use the standard line printer character set. The following page contains an example of this type of print out.

In the print out, all logic symbols are blocks. The logic function is denoted by an appropriate tag within the block, along with module location data. Pin numbers are shown, as well as the amount of loading (number of circuits being driven by an element).

The idea of automated logic diagrams was enormously appealing, since it would reduce the time needed to draw the diagram, and also would produce a quick, simple method of updating and correcting diagrams. Theoretically, the diagrams would also be more accurate.

Three factors were subsequently introduced which caused this idea to be abandoned, at least on a widespread basis. First, the print out itself proved to be inadequate in that the use of standard



Automated Logic Diagram – Sample

line printer characters created confusion in many complex logic structures. An example is the use of the character "I" to indicate an inverting function within a block, and also used as a means of drawing vertical lines outside of a block. Secondly, when logic structures are reduced to blocks one of the most valuable characteristics of a logic diagram is negated; the association of symbol shapes with logic functions. Lastly, reproduction of the print outs proved to be generally poor unless the line printer ribbon was changed frequently and the printer mechanism kept in optimum operating condition.

Because of these drawbacks, engineering decided to cancel the project. The program, however, is still existent, and some departments are using the print outs for internal use. No mass production of these diagrams are currently in progress, nor is there any likelihood that this project will be reinstituted at some later time. Further, hand-drawn logic diagrams will not be available for troubleshooting as part of the standard equipment documentation.

You will, however, be exposed to some "unofficially" drawn logic diagrams, either in a simplified manner, or completely implemented. These diagrams are being used in Technical Manuals and Training documents to clarify logic structures where necessary.

The company's decision to have Test and Maintenance personnel rely heavily on the use of logic equations for troubleshooting has been met by generally wide acceptance. Equations are easier to update, consume less space, and contain the same information as logic diagrams, except for forward references. On very large logic structures, such as found in a central processor, the equations represent a much more usable document than diagrams since they are much easier to work with than a large, combersome set of logic diagrams which would fill many pages.

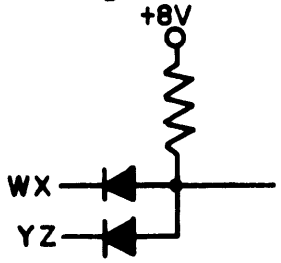
Those who are used to troubleshooting with diagrams are the most resistive to working with equations. This is understandable. However, after becoming familiar with how to read and use the logic equations, they frequently find that equations are just as meaningful as the diagrams. Some logic structures, however, are very complex, and a logic diagram does aid in understanding these complex networks. In the electro-mechanical area, where mechanics are controlled by logic circuits, diagrams are useful. In core memory, where many non-logical functions are performed, diagrams are useful. You will find that some logic diagrams have been generated by either Technical Publications or Technical Training to assist in the understanding of certain structures in these areas.

Whether you prefer to use equations or diagrams is really a moot point since diagrams are not officially available. The ability to read and use the logic equations as published by SDS is the basic ability you must acquire to maintain and understand Sigma equipment. This ability overshadows everything else in importance, since without it you cannot effectively perform your job.

The following information relates to how the Automated Logic System works, how logic equations are produced, as well as wire lists, what they say, and how to use them in maintaining Sigma equipment. This information is very important to you and should be studied carefully.

The symbol "B" to the right of the equality is a standard symbol for a Buffer Amplifier. This symbol is called an "Element Designator" and designates what kind of circuit is driving the function, F. Thus, a Buffer Amplifier is the hardware element being used to generate the function, F. Because F is an output logic term, "B" is an output Element Designator.

The two input terms, WX and YZ, are preceded by dots, or "period" symbols which indicate that WX is an input to an AND-facing diode, and YZ is also an input to an AND-facing diode. Further, it implies that WX and YZ are ANDed together. Schematically:



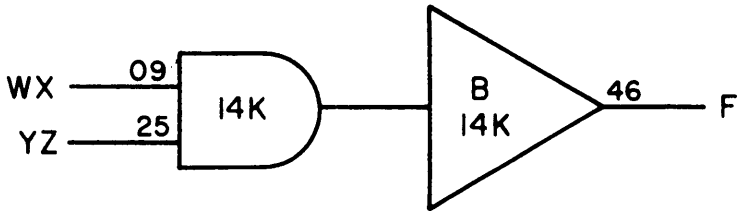
Since the AND symbols (.) precede the input terms in the logic equation, the "." symbol is called an Input Element Designator.

Thus, from the implemented equation a person can find not only the logic function performed, but also how it is implemented.

The physical location of this logic is important to know for trouble-shooting. When the designer assigns the module to a location within the equipment, he will then write the module location and pin numbers beneath the implemented equations in this manner:

```
F  =  B .WX .YZ      (Logic Line)
      14K46, 09, 25  (Pin Line)
```

The Pin Line expresses the module and pins where the logic terms can be found. In this example, "14K" indicates the Buffer and the input AND gate are located in module 14 of chassis (row) K. The number "46" following "14K" indicates that the Buffer output is pin 46. This is where the logic term, F, can be found. The comma symbol is just a separator, and has no logic relationship. The number "09" indicates that the first AND diode can be found on pin 09, and the number "25" indicates that the second AND diode can be found on pin 25. Since WX and YZ are the input terms to these diodes, they can be found on pins 09 and 25. If a drawing were to be shown of this logic structure, it would appear as:



The destination of the logic term, F, is the only important piece of information lacking. This information is not available in the implemented equation, but is available in another document, the Pin List.

When the designer has all of his logic functions defined as implemented equations, he submits them to key punching and inputs this into the computer under the control of the LOTRAN program. The program formalizes his equations into a standard format, and provides the designer with these formalized equations, a load list (pin list) showing how many elements each output term is driving, and an error list showing him any mistakes he might have made in assigning module or pin information, or errors in his syntax.

After several passes through this cycle, during which mistakes are corrected, the LOTRAN program would provide a set of documents which include:

1. Automated Logic Equations
2. Pin List
3. Pin Index
4. Module Map
5. Wiring Verification List (on magnetic tape)
6. Manufacturing Wiring Book

The Wiring Verification List is used by the Automatic Wiring Verification (AWV) test stations to test all point-to-point wiring under computer control.

The Manufacturing Wiring Book is used on the assembly line to perform the actual wiring of the backpanels.

The Automated Logic Equations, Pin List, Pin Index, and Module Map documents are the only documents which are of use to the Customer Engineer, and will be discussed in detail in the following pages.

Automated Logic Equations

The Automated Logic Equations contain all the Logic and Pin Lines that pertain to a functional unit of logic, which could be either a chassis of plug-in modules, or a complete Frame (9 rows) of plug-in modules, depending upon the equipment type.

The Automated Equations are presented in three distinct Sections:

1. Glossary of Element Designators
2. Logic Listing
3. Dictionary

The Glossary of Element Designators is placed towards the beginning of the Automated Equation book, immediately preceding the Logic Listing. It contains definitions for all the Element Designators used in the Logic Listing.

The Logic Listing contains all of the logic and pin lines that make up the functional unit. It is arranged numerically by Line Numbers.

The Dictionary is an alphabetical listing of all output logic terms which provides a cross reference to the appropriate Line Number, which can then be used to find the logic term in the listing. The Dictionary does not define the meanings of logic terms. The Dictionary is located either at the beginning or the end of the equation book.

The following three pages are examples of these three Sections.

CODE	LINE NO.	CHG	LOGIC EQUATIONS / PINS / REMARKS	C/L
1	2 ... 8	9	10 ... 15 ... 20 ... 25 ... 30 ... 35 ... 40 ... 45 ... 50 ... 55 ... 60 ... 65 ... 70	
I	.		AND	
I	*		DIRECT INPUT	
I	CI		CABLE INPUT	
O	+		OR	
O	B		BUFFER AMPLIFIER	
O	-BCD		BUFFERED CABLE DRIVER	
O	-BCR		BUFFERED CABLE RECEIVER	
O	CO		CABLE OUTPUT	
O	-CON			
O	FB		BUFFER FLIP-FLOP (SET)	
O	FF		STANDARD J/K FLIP-FLOP (SET)	
O	FN		NAND FLIP-FLOP (SET)	
O	FR		REPEATER FLIP-FLOP (SET)	
O	-GND		GROUND INDICATOR	
O	-HSM		HIGH SPEED MEMORY	
O	I		INVERTING AMPLIFIER	
O	-LD		LAMP DRIVER	
O	NFF		STANDARD J/K FLIP-FLOP (RESET)	
O	NFN		NAND FLIP-FLOP (RESET)	
O	NFR		REPEATER FLIP-FLOP (RESET)	
O	-NS		NO SOURCE INDICATOR	
O	-TD		TIMING DELAY	
O	-VSP		SPECIAL VOLTAGE	

EXAMPLE - GLOSSARY OF ELEMENT DESIGNATORS

```
CODE | LINE NO.  | CHG | LOGIC EQUATIONS / PINS / REMARKS                                                  | C/L
   1 | 2 3 4 5 6 7 8 |  9 | 10 ... 15 ... 20 ... 25 ... 30 ... 35 ... 40 ... 45 ... 50 ... 55 ... 60 ... 65 ... 70 |
-----+---------------+-----+-------------------------------------------------------------------------------+-----
     | 6105400  MMCW       =B*   +.FUMMC-1.PH5-B                                                         | A
   P | 6105400             12B36, $,$,26,     25,36-23C45T                                               | A
     | 6105402                    +.FUMMC-1.PH4-B.N(NP32.NP33)                                           | A
   P | 6105402              12B$,29,      28,   27                                                       | A
     |                                                                                                   |
     | 6175050  MP19       =FF                                                                           | A
   P | 6175050             03E04,   04-01B25C-03C15C-03D15C                                              | A
     |                                                                                                   |
     | 6175052  NMP19      =NFF                                                                          | A
   P | 6175052             03E05                                                                         | A
     |                                                                                                   |
     | 6175054  S/MP19     =*   +.BCON   .(S/MP19/1)                                                     | A
   P | 6175054           03E03,  03,10X,  24                                                             | A
     | 6175056                  +.GND03E16                                                               | A
   P | 6175056             03E03,17X                                                                     | A
     |                                                                                                   |
     | 6175060  R/MP19     =      .                                                                      | A
   P | 6175060               03E22                                                                       | A
     |                                                                                                   |
     | 6175064  C/MP19     =      .CL-18E40                                                              | A
   P | 6175064               03E01X                                                                      | A
     |                                                                                                   |
     | 6175150  (S/MP19/1) =B     .MIT   .NMITEX   .NMP19                                                | A
   P | 6175150             02E37,46      50,       41,37-09E24T                                          | A
     |                                                                                                   |
     | 6178000  MPP        =B*   +.PH3-4   .CSN   .                                                      | A
   P | 6178000  12E42,$,$,40,50,39X,42-31C19C-31D19C-14F03C-14G03C-19H02T                                | D
     | 6178002                    +.PH5-D   .CSN                                                         | A
   P | 6178002              12E$,28X,     29                                                             | A
     | 6178004                   +.PH7-F   .FAFLMD                                                       | A
   P | 6178004              12E$,43,      44X                                                            | A
     | 6178008              B     .FAFLM   .ASN                                                         | A
   P | 6178008             11E46,41,      40                                                             | A
     |                                                                                                   |
     | 6196000  (MAR+MRQ/1)      =I    .NMRQ   .NMRQ/1                                                   | A
   P | 6196000              07C17,   20,     21,   17-02B11C                                             | A
```

EXAMPLE - LOGIC LISTING

CODE	LINE NO.	CHG	LOGIC EQUATIONS / PINS / REMARKS	C/L
1	2 ... 8	9	10 ... 15 ... 20 ... 25 ... 30 ... 35 ... 40 ... 45 ... 50 ... 55 ... 60 ... 65 ... 70	
	6105202		NMITEX	
	6105204		S/MITEX	
	6105214		R/MITEX	
	6105218		C/MITEX	
	6105400		MMCW	
	6175050		MP19	
	6175052		NMP19	
	6175054		S/MP19	
	6175060		R/MP19	
	6175064		C/MP19	
	6175150		(S/MP19/1)	
	6178000		MPP	
	6196100		NMRQ	
	6196000		(MRQ+MRQ/1)	
	6197000		MRQ/1	
	6196900		NMRQ/1	
	6197580		(S/MRQ/M)	
	6224000		MULC	
	6224002		NMULC	
	6224004		S/MULC	
	6224010		R/MULC	
	6224014		C/MULC	
	6224050		(S/MULC/1)	
	6224500		MUSIC	
	6224502		NMUSIC	
	6224504		S/MUSIC	
	6224508		R/MUSIC	
	6224510		C/MUSIC	
	6240000		MW	
	6240100		NMW	
	6242100		MWB	
	6242200		NMWB	
	6242800		MWH	
	6242900		NMWH	
	6244011		MWN	
	6244017		NMWN	
	6244020		MWN-1	
	6244120		(MWN-FAFLM)	
	6244130		N(MWN-FAFLM)	
	6244050		(MWN-RN)	
	6244060		N(MWN-RN)	
	1014510		O1	
	1014520		NO1	
	6510930		(O1.NO2)	
	6510950		(O1.NO3)	
	6511100		(NO1.NO3)	
	6511000		(NO1.O2)	
	6511200		(O1.O3)	
	6511300		(NO1.O3)	
	6511710		NO1-1	
	1024510		O2	

1 2 ... 8 9 10 ... 15 ... 20 ... 25 ... 30 ... 35 ... 40 ... 45 ... 50 ... 55 ... 60 ... 65 ... 70

Automated Logic Equation Syntax

In the preceding example, showing how a logic listing is constructed for a very simple logic function (F = WX.YZ), we have seen that a logic listing consists of two parts: a logic line and a pin line.

We shall now expand our horizons and take a close look at all the component parts of a logic listing, how logic and pin lines are constructed under a variety of circumstances, how the logic listing relates to a logic diagram, and how to read and interpret any logic listing.

Logic Lines

Logic lines use two component parts: Element Designators and Logic Terms. The Element Designators indicate what hardware is being used; the Logic Terms give the various inputs and outputs a name.

Element Designators

Element Designators are symbols used to denote the individual circuit elements which form the complete logic circuit, and reflect hardware inputs and outputs. Element Designators are categorized into two parts: Standard and Special.

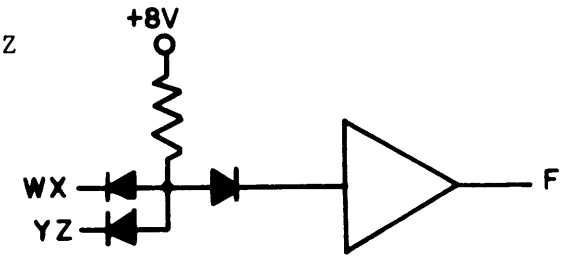
Standard Element Designators - When Sigma was started, designers established a very basic set of Element Designators that were to be common to all Sigma equipment, and were to reflect circuits which were going to be widely used in all Sigma equipment. This Standard Element Designator list is reproduced in all glossaries in the Automated Equations, regardless of whether or not the unit uses those designators. The Standard Element Designators are:

ELEMENT DESIGNATOR	TYPE	DEFINITION
.	I	AND Diode
*(1)	I	Direct Input
+(2)	O	OR Diode
I	O	Inverting Amplifier
B	O	Buffer Amplifier
CI	I	Cable Input
CO	O	Cable Output
FF(3)	O	J/K Flip-Flop Set Output
NFF(4)	O	J/K Flip-Flop Reset Output
FR(5)	O	Repeater Flip-Flop Set Output
NFR	O	Repeater Flip-Flop Reset Output
FN(6)	O	NAND Flip-Flop Set Output
NFN	O	NAND Flip-Flop Reset Output

(1) The Direct Input designator implies that a single input line feeds the active element (Buffer, Inverter, etc.). This designator is important only in the case where several OR nodes are connected together at one common connector pin (or etch connection) and used as an input to an active element. It has no logic significance.

(2) The OR Diode designator indicates that the logic following the symbol goes through an OR-facing diode, viz:

F = B * + .WX . YZ



(3) The "J/K" designation actually refers to the Set Override feature of the SDS 307 or 311 IC flip-flop, and not to the classic J/K mode of operation.

(4) The "N" in "NFF" is the negation symbol in Sigma equations and takes the place of the more familiar "bar" over a term. Thus, if A = 1, then NA = 0.

(5) FR and NFR (Repeater flip-flop) designators are not being used in the Sigma equations. The Repeater flip-flop is a carry-over from the 9-Series equipment, and is not being implemented in the Sigma Series.

(6) FN and NFN (NAND flip-flop) designators are not being used. In the case of DC flip-flops wired from either NAND or NOR elements, the equations will reflect Inverter elements with the proper input gating. Most Sigma DC Flip-Flops are implemented using Buffer Latch circuits.

Special Element Designators - Used to indicate "non-standard" elements (those not defined in the preceding list). As the Sigma line developed, the Special Designators have outgrown the Standard Designators by at least 10 to 1. It is anticipated that many of the Special Element Designators will become Standard. At the present, all Special Element Designators are assigned by individual logic designers. Because of this there may be variations in some of the definitions of Special Designators, therefore, it is a good idea to always check the glossary of element designators on each equation book before using it. All Special Element Designators are preceded by a hyphen (-) symbol. The following list reflects some of the more commonly used Special Element Designators.

ELEMENT DESIGNATOR	TYPE	DEFINITION
-BCD, -CD	O	Buffered Cable Driver
-BCR, -CR	O	Buffered Cable Receiver
-BDS	O	Delay Line Sensor
-CLD, -CD	O	Clock Driver
-CON	O	Special Connection
-DL	O	Delay Line Tap
-FB, -BFF	O	Buffer Latch (Set Output)
-NFB	O	Buffer Latch (Reset Output)
-GND, -GRD	O	Ground Indicator
-HSM	O	High Speed Memory Element
-IDS	O	Inverting Delay Line Sensor
-LD	O	Lamp Driver
-NS(1)	O	No Source Indicator
-OS, -COS	O	Oscillator
-PG	O	Parity Generator
-PS	O	Pulse Shaper
-SW, -SWC	O	Toggle Switch or Relay Contact
-TD	O	Delay Element (fixed)
-VSP	O	Special Voltage
-VSS	O	Special Wiring (Twisted-Pair, etc.)

(1) The No Source Indicator is used if a logic term appears in one logic unit (chassis, frame, etc.) but is actually generated externally. The -NS then indicates that the logic structure which generates that term cannot be found in the current equation book.

Since wire lists and wiring books are generated by essentially the same information which produces the logic equation book, you will encounter logic "equations" which have no logical significance in terms of Boolean functions. Thus, ground and power connections will be shown, and, in core memory, load resistors, core stack drive lines, and other wiring data will appear in equation form. Diagrams, schematics, and other drawings are then necessary to supplement those types of "equations".

Thus, Element Designators (Standard or Special) attempt to define the type of circuitry which is used to produce a logic term. They are either Output (Buffer, Inverter, etc.) or Input (AND-diode, Direct, etc.) oriented. In the equations, the Element Designators appear only in the Logic Lines, never in the Pin Lines.

Logic Terms (signal names)

It has already been discussed that logic symbology in SDS is in a state of flux. It could be said also that the industry as a whole is still uncertain as to whether or not a standard, industry-wide, set of logic symbols should be accepted. So, logic symbology is still an art, not a science, in a sense.

The naming of logic signals is, in that sense, also an art in most companies, including SDS. Many methods of naming signals are used, with valid arguments supporting each method. Some companies have used a hardware-oriented method where logic terms are merely reflections of functional unit and module locations, while others have gone to the other extreme and use everyday English names.

Signal naming in Sigma has been done under a rather informal, word-of-mouth policy. In general, a Sigma signal name is written with two basic considerations in mind:

1. It should be as short as possible, either by abbreviation or truncation of an English name (ST for START, WDT for WATCHDOG TIMER), and;

2. It should have as much association with either the function it is to perform, or, the functions which create it.

Because of the infinite range of logic structures which can be implemented, signal-naming has been reduced to simply what the designer feels is the most suitable name for the signal, guided loosely by these two basic considerations.

In many of the logic terms (alphanumeric and special characters) some characters have been used to represent a common (perhaps logical) function which is independent of what function(s) the term affects or is affected by. The following are most of these common signal name characters:

A. "N" - Logical negation. When the signal "WX" is true, the "NWX" is false, and vice-versa. This could be implemented as:

```
WX  =  B .W .X
NWX =  I .WX
```

or, as:

```
WX  =  B .W .X
NWX =  I .W .X
```

depending upon speed requirements and/or available circuits.

B. "X" - When used as a middle character or suffix character usually means a transfer function. Thus, "AXS" means "transfer S to A"; likewise,

"SXCS" - transfer CS to S
"B31X1" - transfer "one" to B31 (Set B31)
"AX0" - transfer "zeroes" to A (Clear A). Could also be written as "AX".
"BXBR2" - transfer B to B, right 2 bit positions
"SX20" - transfer a hexadecimal 20 to S
"RNXRR0"- transfer RR0 to RN
"NRNXRR0"- do not transfer RR0 to RN

C. "W" - When preceded by a number or numbers, means "ones". Such as "A0004W", meaning "bit positions 00 through 04 of A (register) contains ones". This could also be expressed as "(A0.A1.A2.A3.A4)", and usually is. The "W" is not used very often.

D. "Z" - When used as a suffix character usually means "zeroes". Such as "B1619Z", meaning "bit positions 16 through 19 of B (register) contains zeroes". This could also be expressed as "(NB16.NB17.NB18.NB19)", however, in this case, the "Z" character is more commonly used.

E. "(A-B)" - Denotes an Exclusive-OR function between elements A and B. The "-" sign is used in this form to replace the "⊕" symbol, which is not part of the line printer character set. This could also be implicitly expressed as "(A.NB + NA.B)"

F. "-" - When followed by a single alpha character or numeric characters, denotes a logically identical function. Some examples are:

SXP-2, SXP-3 - These signals are logically identical.
SXP-2 = I .NSXP
SXP-3 = I .NSXP

GX-0,GX-1,GX-2 - These signals are logically identical.
GX-0 = I .NGX
GX-1 = I .NGX
GX-2 = I .NGX

C. "/" - In flip-flop input logic, the "/" symbol is used to separate the input type from the input name. Thus:

S/FAM means "Set FAM"

R/FAM means "Reset FAM"

C/FAM means "Clock for FAM"

F/FAM means "Force FAM" (DC Set)

E/FAM means "Erase FAM" (DC Reset)

When used as a suffix, followed by either a single alpha character or numeric characters, the "/" symbol denotes a logical similarity between it and other logic terms with the same base name. Thus;

DXC/12 = I .NDXC/7 .NDXCM . NDXC/D

DXC/13 = I .NDXC/7 .NDXCM . NDXC/D .NDXC/1

show that DXC/12 and DXC/13 are similar, but not identical, since DXC/13 is affected also by the term NDXC/1, where DXC/12 is not.

An example of the difference between the use of "-" and "/" can be shown with the following terms:

```
NFAIO  =I * + .OU4 .(04.05)
           + .OU6 .OLE
 FAIO  =I .NFAIO
FAIO-1 =I .NFAIO
FAIO/1 =B .FAIO-1 .OU4
```

H. "/ /" - When the "/" symbols are used to enclose a signal name it denotes a cable signal. Thus, the term, "/AHC/" indicates that "AHC" is sent out through the (33-ohm shielded) cable, and is the output of a Cable Driver, and the input to a Cable Receiver. Further, this signal, /AHC/, would have the logic levels of +2VDC (1), and 0 VDC (0).

I. "=" - The equality symbol is rarely used as a part of a signal name, but it has been used in terms such as "(E=1)", meaning, "the E (Register) contains a count of +1".

J. "( )" - Parentheses are used when the signal name is associated with the logic which creates it, rather than what function the term is to affect. These signals are sometimes referred to as "imbedded logic terms", and usually show the Boolean result of a logical operation:

(FAMUL . MIT) = B .FAMUL .MIT

N(B31 . BC31) = I . B31 .BC31

Or, it is used to denote an intermediate logic term as shown below:

S/BC31 = * + .BCON . (S/BC31/1)
+ .FPPN
+ .SFTR2 .B30
+ .FAMUL .PH1-4 .RN

(S/BC31/1) = I * + .NB31 .NBC31
+ .NB30

where the use of "(S/BC31/1)" attempts to show some relationship to the setting of flip-flop BC31.

K. "GND" - When element inputs are grounded, the signal "GRD" name "GND" (or "GRD") is used, followed by the module and pin number where the ground source is. Thus, the signal "GND27C16" indicates that a ground wire from module 27, row C, pin 16, is connected to this point (the pin associated with the signal in the Pin Line). An example is:

```
S/RESET/F  =  * + .RESET-1
              + .GND21E32
```

In this example, the second, unused, OR diode output must be grounded, otherwise the input to the flip-flop will always be true.

L. "CL" - Clock pulses in the various units are usually common to most AC (clocked) flip-flops and are generally referred to simply as "CL" clocks. The equations reflect the clock source in the same manner as ground sources, by including the module and pin number where the clock is wired from. Thus, the clock input to flip-flop, RTZ, would appear as:

```
C/RTZ  =  .CL-18E40
```

which indicates that the clock pulse appearing on the AND diode inpit to RTZ is coming from Module 18, row E, pin 40.

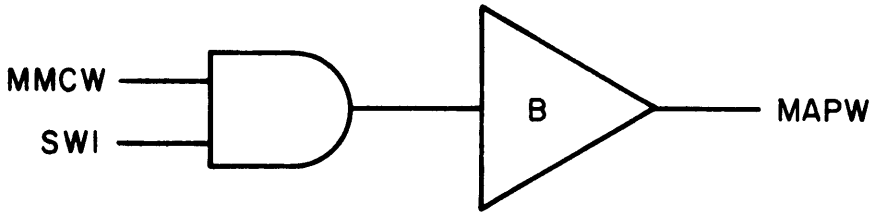
Signal name definitions are not available in the equation books; instead, they can be found in either a Technical Manual or other such document for the equipment.

In you experience with these equations you will find discrepancies in the construction of logic lines, and a violation of one of the above general statements regarding some of these "common" characters. Fortunately, they seem to be relatively small in number, considering the bulk of equations which represent the Sigma equipment line.

So far we have discussed how equation logic lines are constructed using two components: Element Designators, and Logic Terms. As a review, attempt to draw the logic diagrams of the circuits expressed by the following logic lines. The correct diagrams are on the page following the logic line:

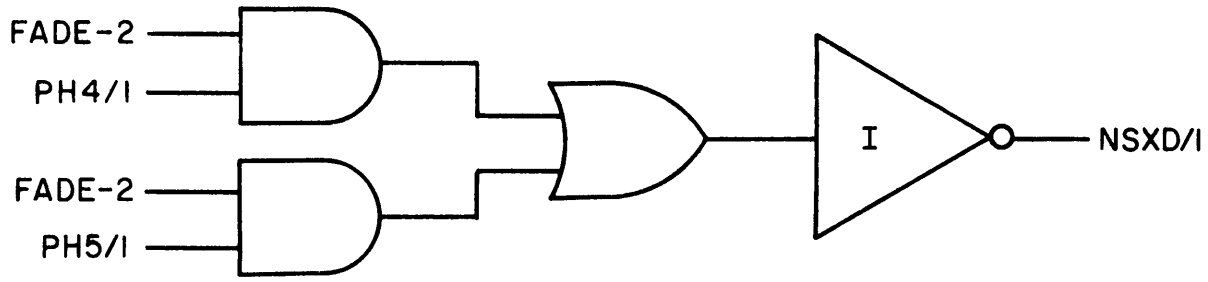
(1) MAPW = B .MMCW .SW1

Correct Diagram for (1):

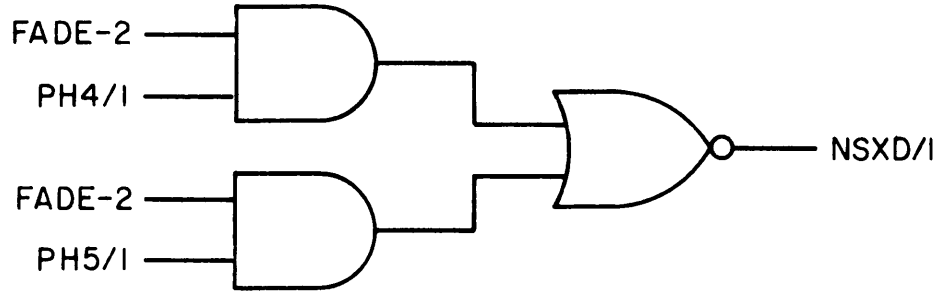


(2) NSXD/1 = I * + .FADE-2 .PH4/1
+ .FADE-2 .PH5/1

Correct Diagram for (2):

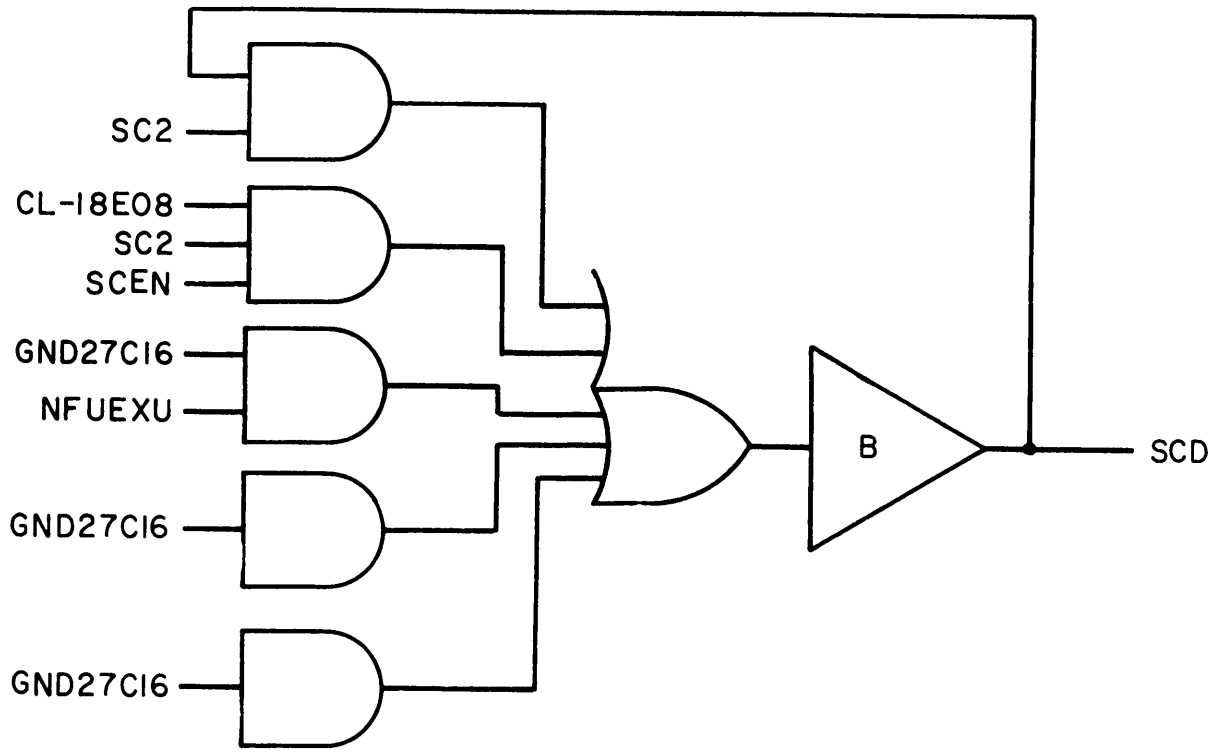


(OR)



(3) SCD = FB * + .SCD .SC2
+ .CL-18E08 .SC2 .SCEN
+ .GND27C16 .NFUEXU
+ .GND27C16
+ .GND27C16

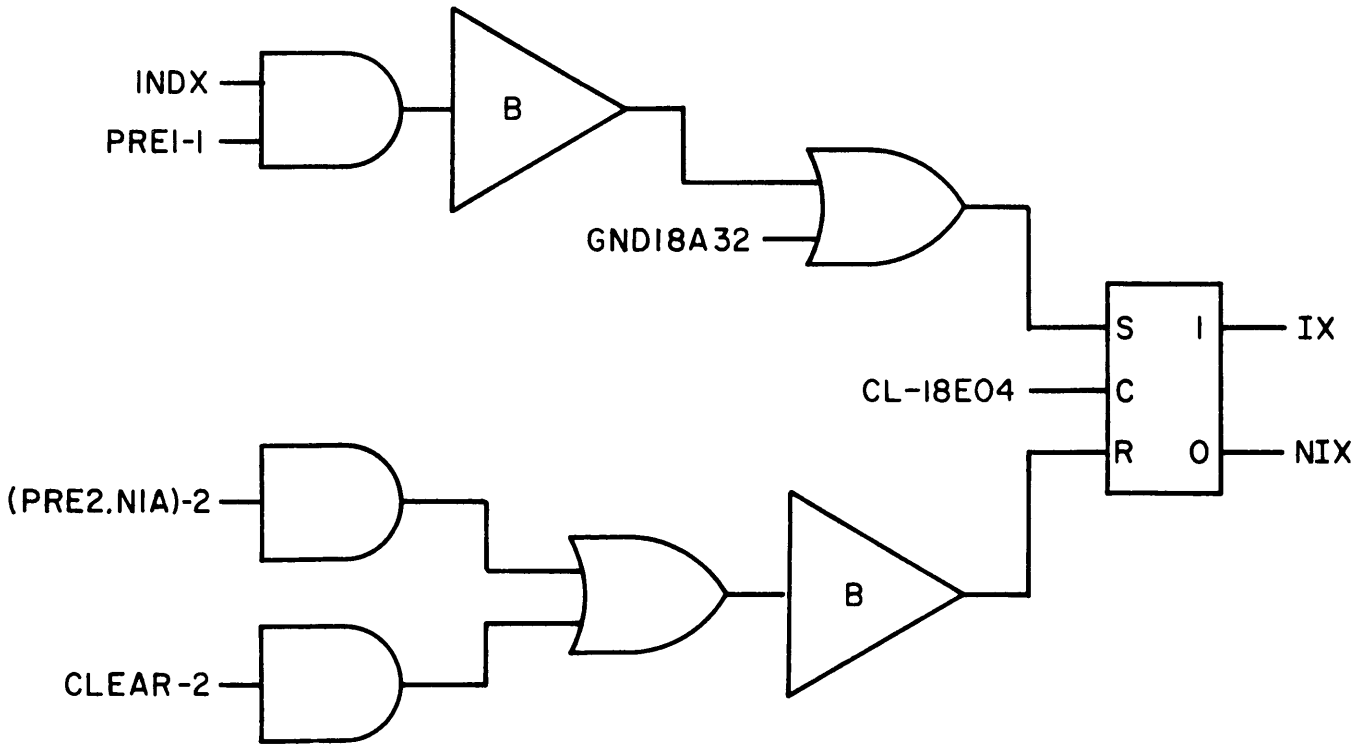
Correct Diagram for (3):



(4)

```
IX   =  FF
NIX  =  NFF
S/IX =  * + .B .INDX .PRE1-1
          + .GND18A32
R/IX =  .B * + .(PRE2 .NIA)-2
             + .CLEAR-2
C/IX =  .CL-18E04
```

Correct Diagram for (4):

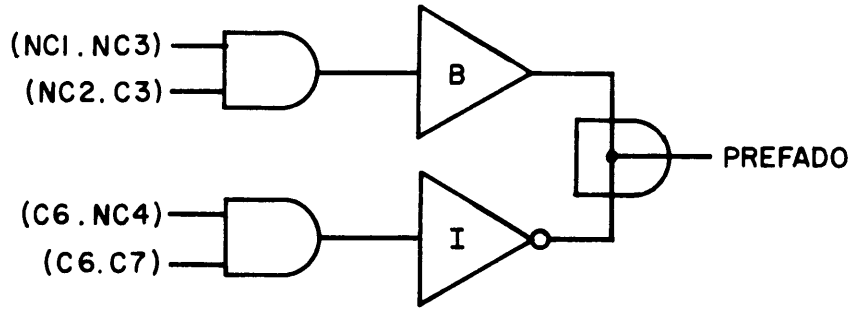


Additional Notes on Logic Lines

When active elements (Buffers, Inverters, etc.) are shown arranged vertically, it indicates that their outputs are wired together to form an AND node. Thus, the following equation:

```
PREFADO  =  B .(NC1 .NC3) .(NC2 .C3)
            I .(C6 .NC4) .(C6 .C7)
```

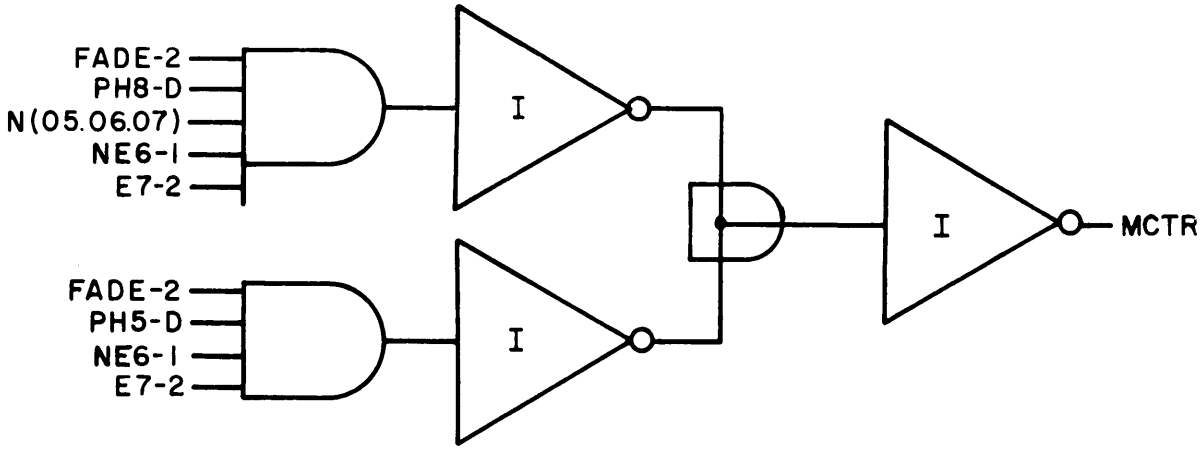
would be drawn to show the Buffer (B) and Inverter (I) outputs wired together to form an AND function:



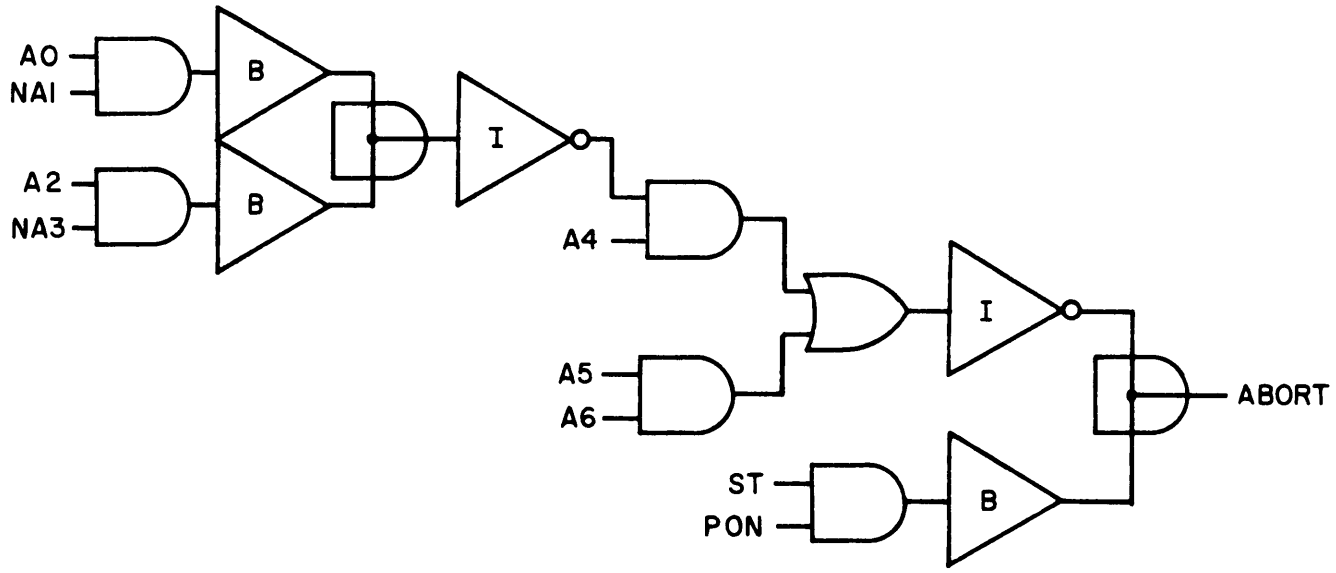
Another example:

```
MCTR  =  I .I .FADE-2 .PH8-D .N(05 .06 .07) .NE6-1 .E7-2
         I .FADE-2 .PH5-D .NE6-1 .E7-2
```

would be drawn as:



Now, as an exercise, how would the following drawing appear as an equation in the format we have discussed? (answer on next page):



```
ABORT  =  I * + .A5 .A6 + .A4 .I .B .A0 .NA1
                                    B .A2 .NA3
          B .ST .PON
```

Or,

```
ABORT  =  I * + .A5 .A6
              + .A4 .I .B .A0 .NA1
                       B .A2 .NA3
          B .ST .PON
```

Unused AND-diodes are always included in the logic lines. This allows designers to keep track of available AND-diodes for future expansion or modification of existing logic structures. It can also be useful in maintenance where it may be necessary to disable (ground) gates for troubleshooting purposes. An example of this would be the equation:

```
N(FAFLAS .FNF)  =  I .FAFLAS .FNF . .
```

showing a 4-input NAND gate with only 2 inputs being used. Remember that open (unused) AND inputs act as a true input.

AND-diodes are also intentionally left open to implement certain logic functions, as in the case of flip-flops using SDS 307 or 311 Integrated Circuits. Since these flip-flops have the Set Override characteristic, it is frequently possible to leave the AC Reset Input AND-diode open and thereby cause the flip-flop to follow the AC Set Input when the Clock falls. It would appear in the logic line in the following manner:

```
  MP19  =  FF
 NMP19  =  NFF
S/MP19  =  * + .BCON .(S/MP19/1)
             + .GND03E16
R/MP19  =  .
C/MP19  =  .CL-18E40
```

The logic lines, then, attempt to represent the logic structures in terms of input and output signals and the logic elements used to form the structure. In theory discussions they represent all the information needed to properly analyze logic functions.

Logic lines, however, are only part of the information available in the Automated Equations. The other information available concerns the physical location of the various elements of the logic lines and also the location of the logic terms. This additional information is contained in the Pin Lines.

Pin Lines

Without the pin lines, troubleshooting with equations would be futile. You can certainly understand how the equipment works with just logic lines, but when it comes time to pull a suspected module or put an oscilloscope probe on a gate somewhere in the logic then you need the information supplied by the pin lines.

First, pin lines represent wiring information and not logic information. Pin line information relates to logic functions using certain conventions or rules.

For each logic line, there is a pin line, situated immediately below each logic line. Pin line information relates only to logic line Element Designators, never to logic terms.

Pin line information always includes:

1. Module and Row of the Element Designator, and;

2. The pin number on the module where the Element Designator input or output can be found (if one is available).

Pin lines may also include wiring information concerning terminator resistor locations (when used), and also indicate when the flat, 100-ohm Ribbon Cable is being used to carry the signal.

Special Character Symbols used in Pin Lines

Certain characters have been set aside which have special meaning when used in a pin line. The following list shows the 6 special characters currently being used and their meanings:

1. "," - The Comma is just a separator, and has no logic or wiring significance.

2. "$" - The Dollar Sign indicates that the Element Designator input or output connection is not available on any of the 52-pin contacts. Therefore, the "$" symbol may indicate that this point may be either an etch connection on the module, or is available on the cable side of a Cable Driver or Receiver module.

3. "X" - The X character indicates that a pin connects to more than one circuit on a module (two or more common inputs).

4. "C" - The C character is used as a suffix to indicate a flat, 100-ohm Ribbon Cable connection which is used for intra- and inter-frame connections.

5 "T" - The T character is used as a suffix to indicate the presence of a terminator resistor (usually 220-ohms connected to +4 VDC).

6. "-" - The Dash symbol is used as a separator for Ribbon Cable and terminator resistor location information.

Examples:

```
OLF  =  B .04 .05 .06 .07
        25J15, 30, 18, 31, 17
```

"25J15" - Module 25, Row J, Pin 15; relates to the Buffer output (B), since B is an Element Designator.

"30" - Module 25, Row J, Pin 30; relates to the first AND-diode input where the logic term, 04, can be found.

"18" - Module 25, Row J, Pin 18; relates to the second AND-diode input where the logic term, 05, can be found.

"31" - Module 25, Row J, Pin 31; relates to the third AND-diode input where the logic term, 06, can be found.

"17" - Module 25, Row J, Pin 17; relates to the fourth AND-diode input where the logic term, 07, can be found.

Notice that the Module and Row was indicated only once, where all of the pins on this line are on the same module. If they weren't, the pin line would reflect it in this fashion:

```
/CNST/  =  -BCD *B.IOPXSTRB .
           29L$, 19, 27L45, 43, 50X
```

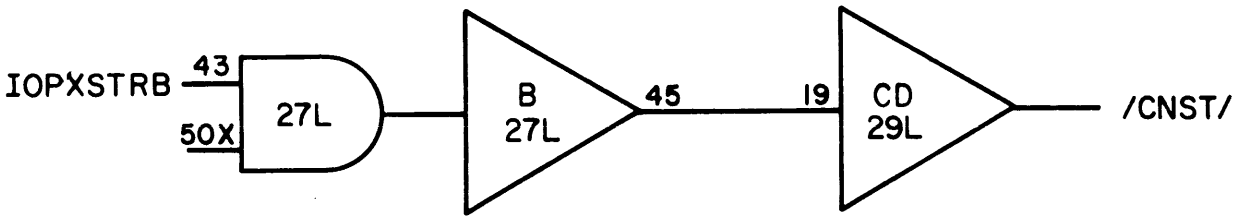
This example brings out several new things. First, the Cable Driver (-BCD) is on Module 29, Row L. The Dollar Sign ($) indicates that the output of the Cable Driver is not available on the 52-pin connector. The "19" indicates that the Direct Input (*) to the Cable Driver is available on pin 19 of Module 29L. Connected to this is a Buffer (B) whose output can be found on Module 27, Row L, Pin 45.

This might imply that there is a wire connecting 29L19 and 27L45, however, there is no indication which guarantees this in the pin line, so, this connection may not be direct as it implies. How these two elements are connected together can only be found in the wire lists, not in the automated equations.

Going on, "43" relates to the first AND-diode input to the Buffer, where the logic term, IOPXSTRB, can be found. This pin is on Module 27, Row L. "50X" relates to the unused AND-diode, and also indicates that this connection is common to at least one other circuit on the module. This pin is also on Module 27, Row L.

It is important to note in this example that the pin line does not indicate where the logic term, /CNST/ can be found. This is true of some logic listings, unfortunately, and should be corrected in the future. To find /CNST/, it is necessary to consult the module data sheet of the Cable Driver. Some logic listings do show where these cable-driven signals can be found on the 14-conductor, 33-ohm cables.

Diagram of /CNST/:



If a logic function must use more than one logic line, then each successive logic line is followed by its own pin line. Each pin line will indicate which module location the following pin numbers relate to, even though all of the pins are on the same module. Thus:

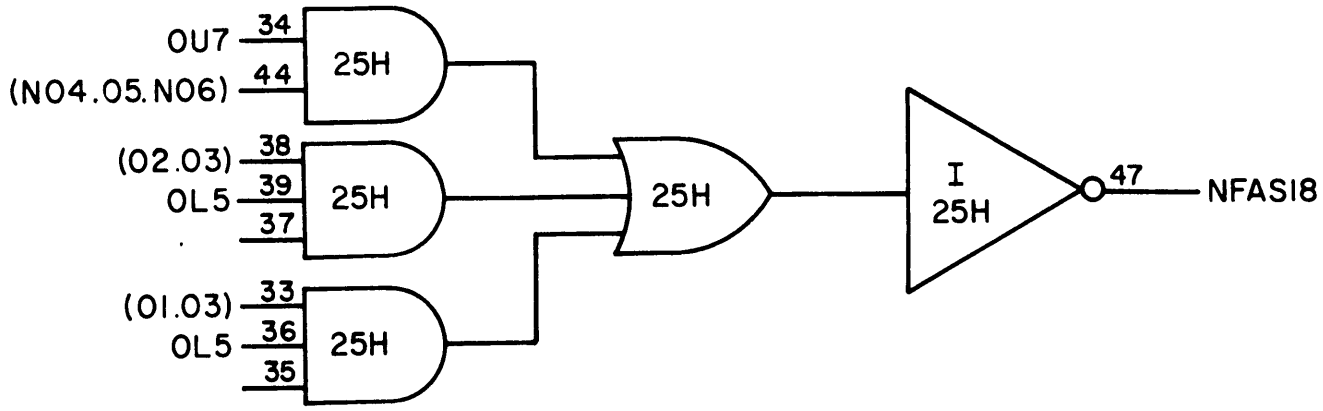
```
EX/1  =  B * + .(FADE .PH6) .DUEND .
      20J01, $, $, 21, 20, 12X
             + .PRE1 .   .
             20J$, 19, 18, 07X
```

where all of the logic is on module 20J. In this example, the OR-diode outputs and the Direct Input to the Buffer are not available at the 52-pin connector as denoted by the "$" symbols.

Now, as an exercise, draw the logic diagram with module and pin information which represents the following equation: (answer on next page)

```
NFAS18  =  I * + .OU7 .(NO4 .O5 .NO6)
        25H47, $, $, 34, 44
               + .(O2 .O3) .OL5 .
               25H$, 38, 39, 37
               + .(O1 .O3) .OL5 .
               25H$, 33, 36, 35
```

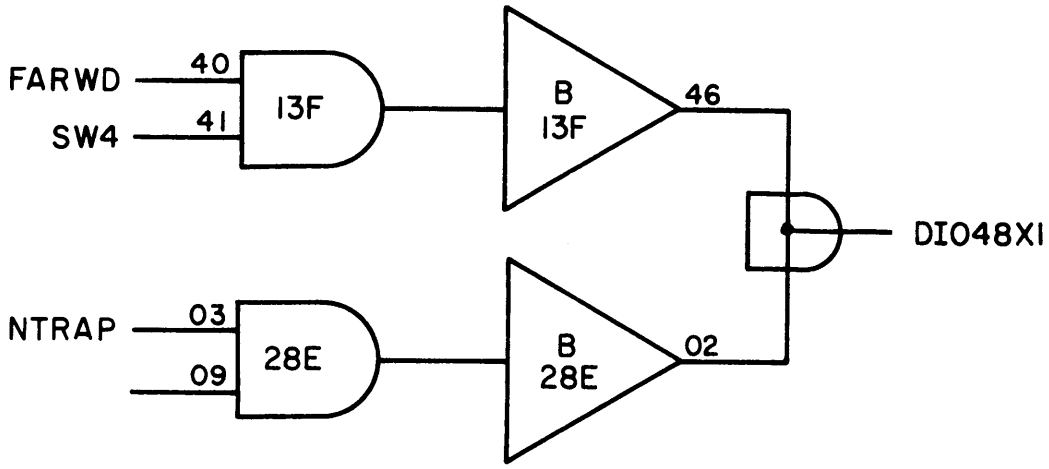
Logic diagram of NFAS18:



Now try:

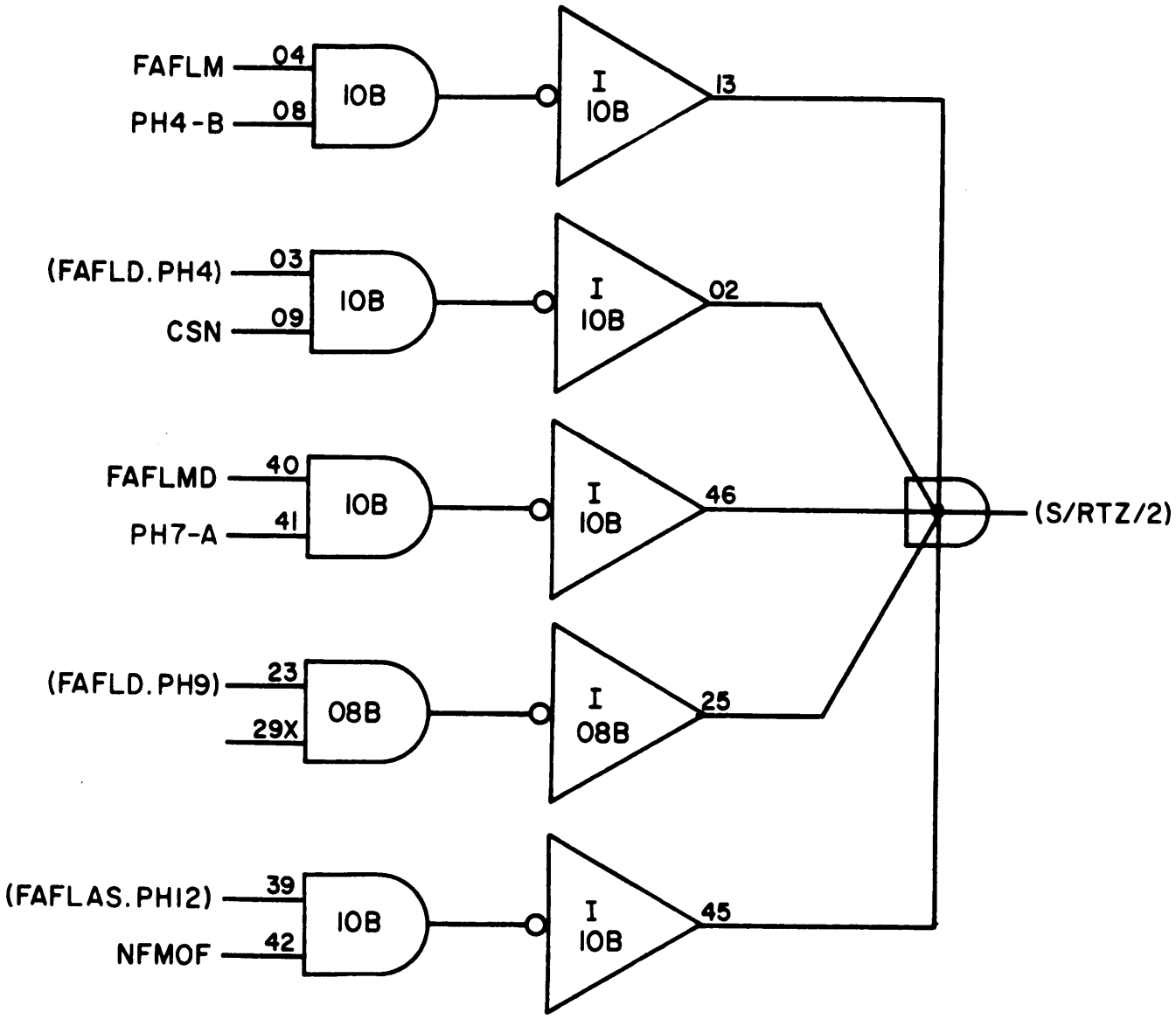
```
DI048X1  =  B .FARWD .SW4
            13F46, 40, 41
               B .NTRAP .
            28E02, 03, 09
```

Logic Diagram of DIO48X1:



Remember, even though it might appear as though there is a direct connection between 13F46 and 28E02, there may not be. The pin line only implies that there is. Certainly, 13F46 and 28E02 ARE connected in some manner.

Now, let's try it the other way around. Construct the logic and pin lines for the following logic structure:


FAFLM
04
PH4-B
08
10B
I
10B
13
(FAFLD.PH4)
03
CSN
09
10B
I
10B
02
FAFLMD
40
PH7-A
41
10B
I
10B
46
(S/RTZ/2)
(FAFLD.PH9)
23
29X
08B
I
08B
25
(FAFLAS.PH12)
39
NFMOF
42
10B
I
10B
45

```
(S/RTZ/2)  =  I .FAFLM .PH4-B
              10B13, 04, 08
              I .(FAFLD .PH4) .CSN
              10B02, 03, 09
              I .FAFLMD .PH7-A
              10B46, 40, 41
              I .(FAFLD .PH9)   .
              08B25, 23, 29X
              I .(FAFLAS .PH12) .NFMOF
              10B45, 39, 42
```

Frequently the pin line contains other information relating to terminator resistors and the use of the flat, 100-ohm ribbon cable for carrying logic signals within and between frames of logic.

If the logic term is wired to a ribbon cable connector for transmission to another part of a frame or to a different frame, the pin line will indicate where the ribbon cable connector is located. It will not, however, furnish the exact routing from the output element to the ribbon cable connector. Thus:

```
SCD-1  =  B .SCD  .
          06B19, 03, 20X, 19-02B23C
```

indicates that the term, SCD-1, which is the output of the Buffer, found on Module 06, Row B, Pin 19, is routed to a ribbon cable connector which is found on Module 02, Row B, pin 23. This information is reflected by the notation, "19-02B23C", where the "C" suffix denotes a ribbon cable connection. 06B19 (SCD-1) may be wired to various points before it finally gets to 02B23, or it may be wired directly to that point. The equations cannot answer as to which method of routing is employed.

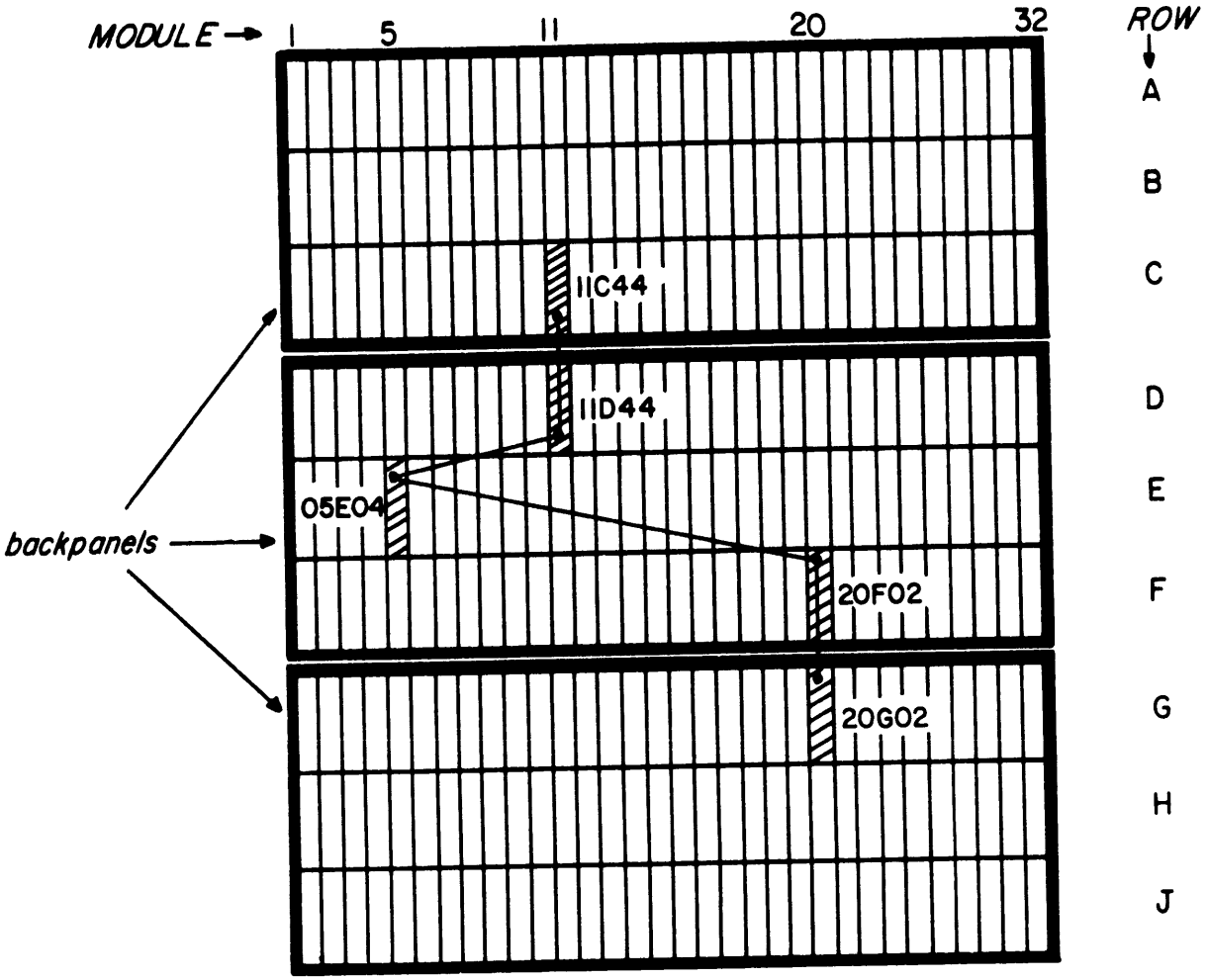
Logic terms may be wired to more than one ribbon cable connector. Thus:

```
SHPC  =  FF
         05E04, 04-20F02C-20G02C-11C44C-11D44C
```

indicates that SHPC, the Set Output of the flip-flop on Module 05E, pin 04, can also be found on 20F02, 20G02, 11C44, and 11D44, all being ribbon cable connectors, denoted by the "C" suffix.

This example brings up another point. The backpanel (where the 52-pin module connectors are available) provides for point-to-point wiring for a maximum of three chassis (rows) of modules. The backpanels are manufactured in this fashion and then are bolted together after they are wired to form a complete frame of logic. Thus, rows A, B, & C would use one backpanel; rows D, E, & F would use another; and rows G, H, & J another. To wire or connect a logic term from one back panel to another, it is necessary to perform this connection after the individual backpanels have been wired and bolted together to form a complete frame. This wiring is accomplished through the use of the flat, 100-ohm ribbon cable.

With this in mind, the above pin line is showing that the logic term, SHPC , is generated at location 05E04, then is wired somehow on the backpanel to 20F02, where it then goes through a ribbon cable to 20G02, located on another backpanel. SHPC is also wired from 05E04 to 11D44 (on the same backpanel), where it then goes through a ribbon cable to 11C44, located on another backpanel. A simplified wiring diagram may clarify this:



(VIEW FROM WIRING SIDE)

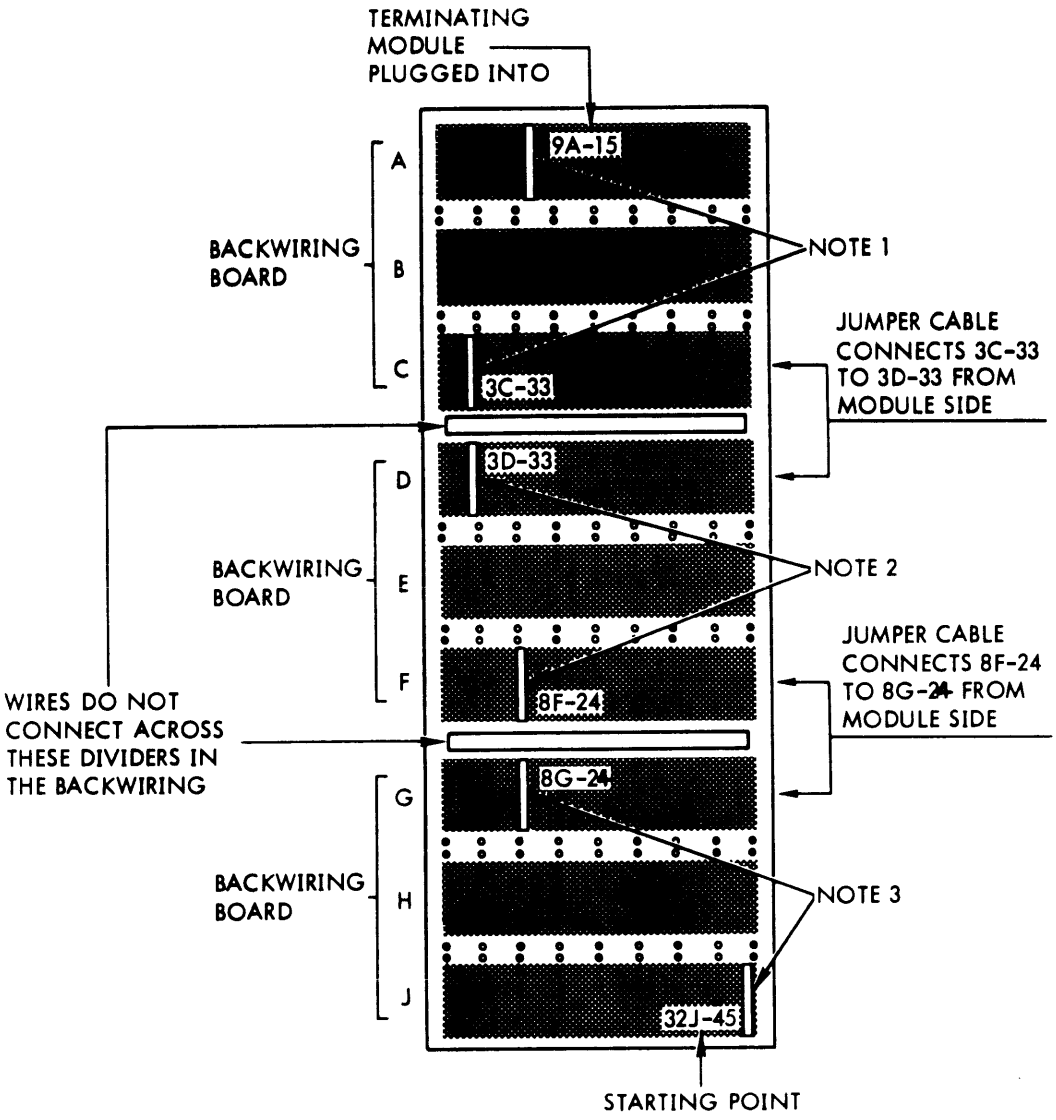
Frequently it is necessary to have a terminator resistor on a signal line to reduce wiring delay. The pin line will indicate the presence of a terminator in this manner:

```
NO1-1  =  B .NO1  .
          04H45, 43, 50X,  45-18J26T
```

where pin 45 of module 04H (NO1-1) is somehow wired (on the same backpanel) to 18J26, where the terminator resistor module is located, as denoted by the "T" suffix. Pin 26 of 18J should then be wired (on the etch) to a 220-ohm resistor returned to +4 VDC, or some other appropriate termination value.

When the terminator resistor is located on another backpanel, then both ribbon cable and terminator resistor information is provided in the pin line. The drawing on the next page reflects this situation, showing the equation as it appears in the logic listing and the wiring routes that would be made.

CODE	LINE NO.	CHG	LOGIC EQUATIONS / PINS / REMARKS	C/L
	4320640		FADW =B* +.0U1 . .	
P	4320640		32J45, $, $, 37, 38, 35X,45-03C33C-03D33C-08F24C-08G24C-09A15T	C
	4320642		+.0U0 .04-1.	A
P	4320642		32J$,40, 39, 41X	A



NOTES : 1. WIRE CONNECTS 3C-33 TO 9A-15
2. WIRE CONNECTS 8F-24 TO 3D-33
3. WIRE CONNECTS 32J-45 TO 8G-24
IN THE BACKWIRING, EACH WIRE MAY CONNECT TO MANY PINS BEFORE REACHING ITS DESTINATION. THE EQUATION DOES NOT GIVE THE ROUTES TAKEN BY REAR WIRES, JUST THE START AND FINISH POINTS ON EACH BOARD.
C INDICATES A CABLE.
T INDICATES TERMINATION.

Backwiring as Shown in the Equation. Termination on the Same Frame

One final note on the logic listings. You will frequently encounter the Element Designator, "NS", meaning "No Source". This indicates that a logic term which appears in the current logic listing (the one you are currently looking at) is generated elsewhere. If the logic listing you are looking at reflects logic for an entire frame, then the generation of that logic term may be in another frame. If the logic listing covers logic in an individual chassis onyl, then the logic term is being generated either in another chassis within that frame, or in another frame, or even in another device.

The pin line will only reflect pin information relating to that logic term as it is used within the unit (chassis or frame) covered by the current logic listing, and will not provide you with information as to the source for the logic term. Thus:

```
RN  =  -NS
       01D39,  39-25E13T
```

only indicates that the logic term, RN, appears on pin 39 of module 01D, and is terminated on pin 13 of module 25E. Where RN comes from is not available.

This concludes the discussion of the Automated Logic Equations. If you have any further questions or do not fully understand any of the information presented here, request clarification from your instructor. The sample page of logic listing may be a source of practice for you. Other, related information on wiring, backpanel construction, etc., appears in the Applications Bulletins in cluded in the rear of this section.

Automated Wire Lists

A wire List for any given unit (chassis or frame) consists of 5 basic documents:

1. Pin List - Arranged numerically by Line Number. Provides a forward reference from an output logic term, showing source, loads, load Element Designator, wire lengths, and termination points;

2. Pin Index - Arranged by Row and Module number. Provides information on all connections made to the 52-pin connector on each module, showing the number of wires on each pin, the destination and source of each wire, the logic term associated with each pin, the Element Designator associated with each pin, and the Line Number of each wire connected to a pin.

3. Module Map - Arranged by Row and Module location. Shows the type of module installed in each of the 32 module loactions in a Row of logic.

4. Manufacturing Wiring Book - Arranged by wiring sequence. Shows the wiring sequence of all point-to-point wiring within a backpanel, and the level (frist or second) of wiring. Useful for manufacturing purposes only.

5. Connection Test List - A magnetic tape listing of all point-to-point wiring within a backpanel. Used for computer-controlled Automatic Wiring Verification (AWV) tests only and is not available to the field.

Only the Pin List and Pin Index documents will be discussed in the following pages. The Module Map needs no discussion. The Wiring Book and the Connection Test List are used only in manufacturing.

Pin List

The following page is a sample of the automated Pin List. The component parts of this list, and how to read and use the list will be discussed in the pages following the sample page.

SOURCE SIGNAL	PIN NO.	LENGTH	SEQ.	TAG	ELEMENT TYPE	WIRE TYPE	LOAD LINE	C/L	ERRO FLAG
1 8	15		21	28	33	37	41	77	
K53									
1532700	20T18	9.6	010	S	B		1532700	A	
	26R38	9.6T	015	L	.		1536500	A	
PR53									
1535500	26R31	9.6	010	S	B		1535500	A	
	20T10	3.0	020	L	.		4510200	A	
	23T45	12.6T	025	L	.		1550120	A	
S53									
1536500	25T06	1.8	010	L	.		1530320	A	
	23T26	1.0	020	L	.		1520120	A	
	22T13	5.2	030	L	.		1490120	A	
	20S15	4.9	040	L	.		1130130	A	
	26R33	2.0	050	S	I		1536500	A	
	29R15	1.6	060	L	.		1136550	A	
	32R25	21.0	070	C	C		1536500	A	
	32M25	13.7	080	C	C		1536500	A	
	12K44	4.5	090	L	.		1570130	A	
	03K44	55.7T	095	T	T		1536500	A	
A54									
1540100	23T31	12.5	010	S	FF		1540100	A	
	27R07	12.5T	015	L	.		1542500	A	
NA54									
1540110	27R02	12.6	010	L	.		1542505	A	
	23T29	1.9	020	S	NFF		1540110	A	
	20T14	14.5T	025	L	.		2011300	A	
1540120-1	23T37	.0T	010	L	*		1540120	E	I
B54									
1540300	14K46	12.6	010	L	.		1560320	A	
	32M21	21.0	020	C	C		1540300	A	
	32R21	2.6	030	C	C		1540300	A	
	27R11	12.0	040	L	.		1546510	A	
	25T31	.7	050	S	FF		1540300	A	
	25T40	48.9T	055	L	.		1530320	A	
NB54									
1540310	25T29	.0T	010	S	FF		1540310	E	I
1540320-1	25T37	.0T	010	L	*		1540320	E	I
C54									
1540500	27R18	12.2	010	S	FB		1540500	A	
	27T40	.7	020	L	.		1531320	A	
	28T39	12.9T	025	T	T		1540500	A	

Pin List Headings

Source Signal - Shows the logic term and Line Number of the term as a cross-reference to the Automated Logic Equations. A suffix of "-1" indicates that one of the loads for that logic line is a Direct Input (as opposed to an AND gate input) to an Active Element (Buffer, Inverter, Flip-Flop, etc.). This flag is used by designer to compute loads.

Pin No. - Shows the module and pin numbers to which the logic term is wired.

Length - Shows, in inches and tenths of inches, the length of wire used from the pin shown under "Pin No." . "T" indicates the total length of wire used to connect the logic term to the various pins.

Seq. - Shows the sequence of wiring, where the smallest number is the start of the wiring string, and the largest number is the end of the wiring string.

Tag - Shows the relationship of an Element to the wiring string:

"S" - Source of the signal. There may be more than one source, as in the case of active elements whose outputs are wired together.

"L" - Load for the signal, usually either an AND-diode input or a Direct input.

"C" - Ribbon Cable connection .

"T" - Terminator resistor; the point in the wiring string where the terminator resistor is connected; not necessarily at the end of the string.

"V" - Voltage connection (+8, -8, +4VDC).

"H" - Used by the Automatic Wiring Verification (AWV) tester only to suppress special wiring tests.

"D" - Diode wired in series in the wiring string; used in core memory for the temperature-sensing diodes.

"*" - connection; usually a ground wire strap.

You may encounter other Tag characters as the assignment of Tags is not standardized. The "L", "S", and "T" Tags will be the ones you will be most concerned about since they relate to the bulk of the logic.

Element Type - Shows the Element Designator (as defined in the Automated Logic Equation glossaries) used as the source or load to the line.

Wire Type - 28 AWG is assumed. When unique wiring is used, other than with 28 AWG it will be called out in this field. The buses which come from power supplies are soldered to certain power pins on the inside laminations of the backpanels (+8, -8, +4 VDC). These connections will have a call out of "ETH". Coaxial cables, used for clock transmission, is labelled, "COA".

Load Line - Shows the correspondong Line Number of all segments in the wiring string. These can be used to find the logic term name associated with a particular input.

C/L - Change Letter; shows individual revision status.

Error Flags - Shows any errors which may appear in the line:

"I" - No connection to this pin (note in this case that the wire length is always shown as ".0T").

"P" - Illegal Pin Field (should never appear in the final, released versions of the Pin List).

Referring to the sample page of a Pin List, let's analyze a portion of it:

K53 is the output of a Buffer (source) on module 20, row T, pin 18. It drives an AND-diode (load) on module 26, row R, pin 38, through a 9.6-inch wire (28 AWG). To relate this to the Automated Logic Equations, you would look in the LOAD LINE column for the Line Number corresponding to the input AND-diode. The Line Number is 1536500. This Line Number can then allow you to find the equation in the Automated Logic Equations where K53 appears an an input:

```
  1536500        S53  =  I * + .PR53 .K53 .SXK-41
P 1536500             26R33X, $, $, $, 38X, 08X, 33X-32R25C-32M25C-03K44T
```

Remember that the Automated Logic Equations are arranged by these Line Numbers. Looking again at the sample Pin List, we can see that the logic term, K53, is only driving one AND-diode input, and that is an input which generates the logic term, S53 (from the equations). K53 is not terminated, nor is it connected to any ribbon cable.

Let's see how the Pin List can be useful in troubleshooting a problem in which the information supplied by the Automated Logic Equations is insufficient.

In diagnosing a machine failure you have encountered an interval where a flip-flop called B54 (bit 54 of Register B) is supposed to set. Up to this time you have been using the Automated Logic Equations to scope certain points in the logic as you single-clock your way through a failing instruction. The logic for B54 is given below:

SDS
SCIENTIFIC DATA SYSTEMS
SANTA MONICA CALIFORNIA

SIGMA 7 CPU FRAME 2

159
131972-001 G
11/29/67

CODE	LINE NO.	CHG	LOGIC EQUATIONS / PINS / REMARKS	C/L
	1540300		B54=FF	A
P	1540300		25T31,31-32R21C-32M21C	A
	1540310		NB54=NFF	A
P	1540310		25T29	A
	1540320		S/B54=*+.S54.BXSF-4 +.B55.BXBL1-4 +.B52.BXBR2F-4	A
			25T37,$,03,08X, $,24X,39X, $,50,41X	A
			+.GND25T16. +.GND25T16. +.GND25T32. +.GND25T32.B54	A
			25T$,09X,07, $,18X,11, $,38X,47, $,33X, 40X	A
	1540330		R/B54= .BXF-4	A
P	1540330		25T02X	A
	1540340		C/B54= .CL-32P38	A
			25T01X	

Using the scope, you put the probe on 25T31 (the Set Output) and discover that during this time interval B54 is not setting when it should be.

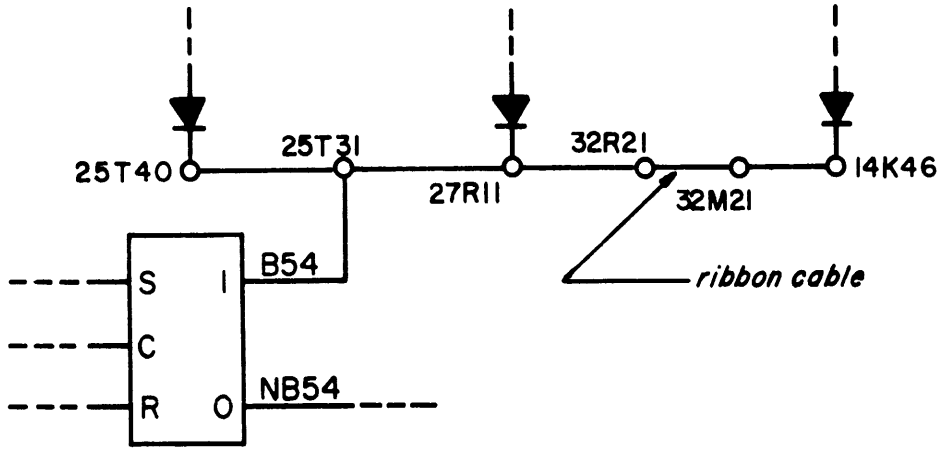
Your next step would be to see if the required inputs to the AC Set Input logic are true. Looking at the equations we see that the Set Input (S/B54) logic has 7 input AND gates which are ORed at the Set input. Only three of these gates are being used; the other four have been grounded. Notice that there is a Direct Input to the Set Input, denoted by the asterisk (*), and that it is available at pin 37 of 25T. Therefore, rather than immediately looking at the appropriate AND gate, we can make a quick check at the Direct Input node to see if this point is at +4 VDC at the proper time. This point should be true when the clock pulse (appearing at the Clock input) goes false. So we connect a probe to 25T37 during the time interval prior to the clock and see that it is in fact true when the clock goes false.

This procedure has eliminated the possiblity of a bad input to the flip-flop. The flip-flop itself is now suspect, and the next logical step would be to replace the module. In a majority of cases, this would be the correct solution to the problem; a faulty flip-flop. But, let's say that after replacing the module you find that B54 still does not set. What now? Replace the module again? Well, its a great temptation when you have spare modules and are getting desperate, but the probability that two of the same modules having the same problem in them is very low. It is far more probable that there is something on the Set Output line of B54 which is keeping the line at 0 VDC, or ground potential.

At this point you look back to the logic equations for help. The equations indicate that the Set Output line is routed somehow to a ribbon cable on 32R21, and goes from there to another backpanel, to module 32M, pin 21, but thats hardly sufficient information. True, you could go pull the ribbon cable out of 32R and see if that will allow the Set Output to go true, but ribbon cables are known to have an open much more frequently than being shorted to ground. So pull the cable from 32R. If the Set Output can now go true, then you either have a problem in the ribbon cable or somewhere beyond there. If the Set Output does not go true, then the problem is somewhere in the backpanel where B54 is located. Either way, you have just run out of information. It is time to drag out the Pin List.

To find B54 in the Pin List, write down the Line Number for the Set Output of B54 (1540300). The Pin List is also arranged by Line Numbers. The equations being used cover the Sigma 7 CPU, Frame 2. So, you will need the Pin List that also covers frame 2. Having gotten it, you look down the first column on the left, under SOURCE SIGNAL, and find Line Number 1540300 and, above it, the logic term, B54. (See the sample Pin List)

Let's analyze the wiring scheme. The source is 25T31 (the Set Output of B54). The wiring string shows that one of the loads is an AND-diode on 25T40, on the same module as the flip-flop, therefore, it is not suspect (you've replaced that module). In the other direction there is another AND-diode load on 27R11, and another on 14K46 which is reached through a ribbon cable connecting 32R21 and 32M21 (rows K, L, and M are using one backpanel; rows R, S, and T are using another). To visualize the wiring string:



Now, either there is a:

1. Short to ground on module 27R, pin 11, or module 14K, pin 46, or;

2. Short to ground somewhere in the ribbon cable, or;

3. Short to ground somewhere in one of the wiring string segments, or;

4. Miswire, causing OVDC to be wired to one of the pins on the wiring string.

Points 1, 2, and 3 are the most probable causes. Point 4 is common in manufacturing, but infrequent in the field. To find if modules 27R or 14K is the culprit, unseat these modules and see if B54 is allowed to Set. If it does, plug one of the unseated modules back in and again check B54. If it still sets, then plug the other module back in (it should be the bad one) and see that B54 cannot be Set. If unseating these modules did not remove the problem, then it will probably be necessary to get a VOM and check for shorts somewhere in the wire string, since we have already checked the ribbon cable.

In this hypothetical problem we have seen how the Pin List is used and when it is used. We saw the limitation of the Automated Logic Equations to furnish forward references, and the method of cross-referencing from one to the other.

Had the hypothetical problem been caused by a miswire there is another document available which could be useful. It is the last document we will discuss in this section, and is called the Pin Index.

Pin Index

The Pin Index is oriented around individual modules. It shows all the wiring connected to a given module. We shall discuss the Pin Index and its component parts, and how it is useful in troubleshooting.

The following page is a sample Pin Index.

FROM	PIN (COUNT)	TO	SOURCE LINE NO.	ELEM. TYPE	SOURCE SIGNAL NAME	REFERENCE LINE NO.
	00(0)					
32P38	01(1)	24T01	3250580	.	CL-32P38	1520340
24T02	02(2)	28T01	2900400	.	BXF-4	1520330
	03(1)	23T40	1546500	.	S54	1540320
	04(1)	23T30	1526500	.	S52	1520320
28T05	05(2)	23T24	1556500	.	S55	1550320
	06(1)	23T26	1536500	.	S53	1530320
	07(0)					
24T08	08(2)	28T07	2936400	.	BXSF-4	1520320
	09(1)	25T16	4783200	.	GND25T16	1520325
	10(0)					
	11(0)					
	12(0)		1520320-1	*		1520320
	13(0)					
	14(0)					
	15(0)					
25T09	16(2)	25T18	4783200	-GND	GND25T16	4783200
	17(0)					
25T16	18(1)		4783200	.	GND25T16	1520325
26R37	19(2)	25T26	1530300	FF	B53	1530300
	20(0)					
	21(0)		1530310	NFF	NB53	1530310
	22(0)		1550310	NFF	NB55	1550310
26R11	23(2)	24T36	1520300	FF	B52	1520300
25T27	24(1)		1550300	.	B55	1540320
	25(0)		1520310	NFF	NB52	1520310
25T19	26(2)	25T43	1530300	.	B53	1520320
27R37	27(2)	25T24	1550300	FF	B55	1550300
	28(0)		1530320-1	*		1530320
	29(0)		1540310	NFF	NB54	1540310
	30(0)					
27R11	31(2)	25T40	1540300	FF	B54	1540300
25T33	32(2)	25T38	4783300	-GND	GND25T32	4783300
	33(1)	25T32	4783300	.	GND25T32	1520325
	34(0)					
	35(0)		1550320-1	*		1550320
28T35	36(1)		1560300	.	B56	1550320
	37(0)		1540320-1	*		1540320
25T32	38(1)		4783300	.	GND25T32	1520325
28T43	39(2)	24T39	2910400	.	BXBL1-4	1520320
25T31	40(1)		1540300	.	B54	1530320
28T44	41(2)	24T41	2924400	.	BXBR2F-4	1520320
	42(0)					
25T26	43(1)		1530300	.	B53	1550320
24T27	44(1)		1510300	.	B51	1530320
	45(0)					
24T40	46(1)		1500300	.	B50	1520320
	47(0)					
	48(0)					
24T49	49(0)	26T49	8300800	V	P4VT	8300830
24T36	50(1)		1520300	.	B52	1540320
24T51	51(0)	26T51	8301800	V	P8VT	8301830

Along the top of the sample Pin Index sheet is the following information:

DRAWING NO. - Shows the engineering drawing number assigned to this Pin Index.

PROG - The program routine which is used to print out the Pin Index; "PNIND".

TYPE - The type of document; "PIN INDEX".

MODULE - The physical module location to which this page of Pin Index applies.

TYPE - The type of module in this location; "FT17".

Within the listing are these headings:

FROM - Where a wire is coming from that is connected to the pin number shown at the right.

PIN (COUNT) - The 52 pin numbers, 0 through 51. The number in parathesis indicates the number of wires that should be found on the pin (0, 1 or 2). When the unit is manufactured a maximum of two wires should be on a pin. There is room for one more wire to be wire-wrapped to the pin; this space is reserved for future revisions to the unit.

TO - Where a wire is going from the pin shown to the left.

SOURCE LINE NO. - Refers to the Line Number of the Source Signal.

ELEM. TYPE - The Element Designator denoting the type of circuitry that is found on this module to which the pin connects. The Element Designators are those symbols defined by the Automated Logic Equations wgich cover this unit.

SOURCE SIGNAL NAME - The name of the logic term appearing on the pin.

REFERENCE LINE NO. - If the Element on the module to which the pin is connected is an output element, then the Reference Line No. is the same as the Source Line No., i.e., an output element is a source element. If the Element on the module to which the pin is connected is an input element, the Reference Line No. refers to the circuit to which the pin and Source Signal is an input.

An example of the difference between the Source Line No. and the Reference Line No. can be seen by looking down the Reference Line No. column and noting how many times the Line No. 1520320 appears. It appears 7 times, each time to a different input element (S52, BXSF-4, B53, etc.). From the Automated Logic Equations you would find that the Line No., 1520320 refers to the AC Set Input to flip-flop, B52. Therefore, all 7 of these input elements are used in the set input to that flip-flop. The Set Output of B52 appears on the sheet and both the Source Line No. and the Reference Line No. are 1520300.

The Pin Index is fairly self-explanatory, and is used more in manufacturing than in the field, since it is an obvious aid in finding miswires. For instance, if, back on our hypothetical problem, where B54 would not set, and we used the Pin List to solve the problem, the real problem was a miswire, we could have used the Pin Index to find the miswire by checking the number of wires on the pins which connected the various points of the output wiring string for B54 against the number of wires shown for thos pins in the Pin Index.

As an exercise, you might compare the wiring on pins 31 and 40 of the sample Pin Index against the sample Pin List to get a better idea of how these two documents are related.

We have just discussed three documents which form the "core" of all other equipment documentation. The ability to use these documents quickly and correctly is one of the most important troubleshooting skills you will learn.

In some of the courses you may attend at the Technical Training Center on Sigma there will be "simplified equations" used in the logic analysis of the equipment. These equations do not reflect implementation, only Boolean functions, and are used solely for quicker understanding of logic functions and information flow when the use of the Automated documents cause considerable delay in going through these functions the first time. Since these Automated documents are the source for all other implementation documents, their correctness should be assumed whenever other documents make contrary statements.

The following pages of this Section are Applications Bulletins which relate to many of the aspects of implementation, wiring, and other hardware principles of Sigma equipment. They should be studied thoroughly. Some parts of these Bulletins were written for designers but contain information useful to you in the field.

MAINTENANCE DOCUMENTS

SECTION VI

MAINTENANCE DOCUMENTS

Maintenance documents comprise the paperwork necessary to learn and maintain equipment, specifically Sigma equipment. They exist in many forms and are produced by many different departments. The following information relates to the different documents you will be using to learn and maintain Sigma equipment from a technical standpoint. Other documents, relating to the administrative duties you will undertake, will be covered by other departments within Customer Service. These documents include Time Cards, Policies and Procedures, Customer Service Reports, Engineering Orders, etc.

The seven basic types of documents which will be discussed are:

1. Reference Manuals
2. Technical Manuals
3. Tek-Tips
4. Engineering Drawings
5. Diagnostics
6. Installation documents
7. Training documents

Reference Manuals

Reference Manuals are prepared by Programming Publications and are distributed by the Publications Stockroom on receipt of an approved Literature Request Form (SDS 267).

Reference Manuals contain all the information necessary to program and operate a particular device and usually include a list of operating characteristics. As such, they represent a powerful maintenance tool, and should be a part of any equipment documentation. Familiarity with the Reference Manual for a device is an important part of efficient maintenance.

Technical Manuals

Technical Manuals are prepared by Technical Publications and are distributed by the Publications Stockroom on receipt of an approved Literature Request Form (SDS 267.)

Technical Manuals contain Theory of Operation, operating characteristics, schematics, logic diagrams, and other explanatory drawings. They may have Illustrated Parts Breakdown (IPB's) drawings and parts lists. They usually do not include the Automated Logic Equations, preferring to use "simplified" equations in discussing logic structures within the device. Most Technical Manuals contain a glossary of logic terms found in the Automated Logic Equations.

Tek-Tips

Tek-Tips are prepared and distributed by Customer Service Product Support Engineering to all Customer Engineers, and to all customers who maintain their own Sigma Systems. Each district office usually has a master file of all valid Tek-Tips.

Tek-Tips provide quick response to problems encountered on equipment and attempt to provide all Customer Engineers with information relating to equipment on a real-time basis. Besides indicating problems and corrective actions, Tek-Tips frequently contain literature lists, parts lists, and other supporting information to help the Customer Engineer maintain equipment. It is essentially a technical document relating to specific equipment, and is not intended to transmit administrative notices except in the case of Engineering Order information, how to fill out and place maintenance decals, etc.

All Customer Engineers are encouraged to voice their problems encountered with equipment through their district offices to Product Support, who will analyze the problem, attempt to resolve it (if you did not), and publish a Tek-Tip with the problem and resolution.

A sample Tek-Tip, relating to Engineering Drawings available on Sigma Equipment, is on the following page.

CUSTOMER SERVICE

TEK TIP NO. 65-50-39

Date November 13, 1967

Ref. E.O. No.

Subject:
Assembly, Maintenance Documents for Sigma Equipment

Related Model Numbers:
All

Distribution:
All

Void After:

Technical Discussion:

Assembly, Maintenance Documents are generated by Product Support Engineering to provide a list of documents which are considered necessary to maintain a particular piece of equipment. All of the documents listed on each Assembly, Maintenance Document must be shipped with the equipment. Assembly, Maintenance Documents for CPU's will include documents for options to the CPU. Peripheral Equipment will usually have two assembly, Maintenance Documents, one for the controller and one for the equipment.

Attached is a list showing the document numbers of all Assembly Maintenance Documents generated to date. A blank in the Assembly, Maintenance Document column indicates that the document does not exist. This Tek Tip will be updated periodically to include documents generated since the last revision.

Attachments:

Prepared By: Evan Bell Date: 11/9/67

Approved: Evan Bell Date: 11/13/67
Product Support Engineer

Approved: Date: 11-13-67
Manager, Product Support Engineering

LIST OF ASSEMBLY, MAINTENANCE DOCUMENTS FOR SIGMA

MODEL	MODEL DESCRIPTION	TOP ASSEMBLY	ASSEMBLY MAINTENANCE DOCUMENTS	NOTES
8001	Sigma 2 CPU	131076	134958	Also Covers Models 8011, 8012, 8013, 8014, 8020, 8023, 8070, 8071, 8091 Controller, 8092 Controller.
8021	Interrupt Control Chassis	117330	134870	Also Covers Model 8022
8050	Ext. Memory Adaptor II	134893		
8051	4K Memory	132712	134869	Also Covers Model 8053
8054	Ext. Memory Adaptor I	134877	139861	
8091	Keyboard Printer (KSR)	133182	137456	
8092	Keyboard Printer (ASR)	130978	136354	
8201	Sigma 5 CPU	117282	145206	Also Covers Models 8211, 8213, 8214
8216	Additional Register Blocks	130071	134873	
8218	Floating Point	134099		
8221	Interrupt Control Chassis	117330	134870	Also Covers Model 8222
8251	4K Memory	132456	134874	Also Covers Models 8252, 8256
8255	Two-Way Memory Access	129463	134875	
8257	Six-Way Memory Access	130625 130626	135383	
8270	External Interface	137086		
8271	Multiplexing IOP	117610	135384	Also Covers Model 8272
8285	Selector IOP	117620	145680	
8291	CFE-3 Control	139237		
8292	CFE-3 Multiply-Add	139228		
8401	Sigma 7 CPU	117307	134872	Also Covers Models 8411, 8413, 8414, 8415, 8418
8416	Additional Register Blocks	130071	134873	
8419	Decimal Arithmetic	117613	134871	

MODEL	MODEL DESCRIPTION	TOP ASSEMBLY	ASSEMBLY MAINTENANCE DOCUMENTS	NOTES
8421	Interrupt Control Chassis	117330	134870	Also Covers Model 8422
8451	4K Memory	132546	134874	Also Covers Models 8452,
8457	Six-Way Memory Access	130625 130626	135383	
8471	Multiplexing IOP	117610	135384	Also Covers Model 8472
8485	Selector IOP	117620	145680	
8491	CFE-3 Control	139237		
8492	CFE-3 Multiply-Add	139228		
8495	System Supervisory Console	127418	135795	
7010	Keyboard Printer (KSR)	117401	136290	
7010	KSR Controller	117402	136289	
7020	Keyboard Printer (ASR)	130978	136354	
7020	ASR Controller	145914		
7060	Paper Tape System	-	-	See 7061.7062.7063.7064
7061	Paper Tape Controller	117447	136355	
7062	Paper Tape Reader	127708	136356	
7063	Paper Tape Punch	127776	136357	
7064	Paper Tape Spoller	117455	136353	
7120	Card Reader 400CPM	124796	137454	
7120	Card Reader Controller	124777	135768	
7140	Card Reader 1500CPM	134359		
7140	Card Reader Controller	135216		
7160	Card Punch 300CPM	137418	137470	
7160	Card Punch Controller	124651	135767	
7201	Medium Speed RAD Controller	135743	136360	
7202	Storage Unit .75M Bytes	123084	139062	
7204	Storage Unit 3M Bytes	123086	136358	

MODEL	MODEL DESCRIPTION	TOP ASSEMBLY	ASSEMBLY MAINTENANCE DOCUMENTS	NOTES
7321	Magnetic Tape Controller	123095	136633	
7322	Magnetic Tape Unit 75ips	123103	137453	
7323	Magnetic Tape Unit 150ips	132979		
7361	20KC M.T. Controller	136967		
7362	20KC M.T. Unit	137003		
7365	BCD Feature	137340		
7371	60KC Tape Controller	134049		
7372	60KC Tape Unit 75ips	133703		
7374	Packing Feature	135786		
7440	Line Printer 600 LPM	123746	134959	
7445	Line Printer 1000 LPM	123737 123577	137457	
7530	11" Plotter	137783		
7530	Plotter Controller	137762		
7531	30" Plotter	137788		
7550	Keyboard Display	133452		
7611	Communication Controller	133905		
7613	Line Interface Unit	133985		
7617	Telegraphic Interface	136614		
7618	Automatic Dialing Unit	139107		
7900	Device Subcontroller	133021	137455	
7901	Perepheral Equipment Tester	132728	139522	
7910	Analog Output Controller	138209		
7914	Analog Input Controller	138208		
7922	Analog and Digital Adaptor	138212		
7929	IOP Digital Controller	138213		
7930	Digital I/O Adapter	138214		

MODEL	MODEL DESCRIPTION	TOP ASSEMBLY	ASSEMBLY MAINTENANCE DOCUMENTS	NOTES
7931	Digital I/O Expansion	138215		

Engineering Drawings

Engineering drawings are prepared by Development Engineering and Drafting, and are distributed by Data Control on receipt of a Reproduction/Drawing Pull Request Form (SDS 171). These drawings are available in either blue-line, Xerox, or multilith form. A drawing printed on pink paper indicates that the drawing is engineering-released and is not to be used for manufactring purposes. When the drawing becomes manufacturing-released, it appears on white, or blue, paper.

Engineering drawings include the following:

1. Master Drawing (Top Assembly) List (MDL) - Lists all hardware assemblies by drawing number, and also lists all engineering documentation (equations, wire lists, etc.) by drawing number. This is usually the first engineering drawing produced on new devices.

2. Automated Logic Equations - Shows all logic in implemented form with module and pin information for each logic term (See Section V).

3. Automated Wire Lists - Includes Pin List, Pin Index, Wiring Book(s), Module Map, and Connection Test List. (See Section V)

4. Module Location Chart - Shows all module locations within a unit and the type of module in each location. Also shows modules which are plugged into the chassis as part of a harware option.

5. Installation Drawings - Provides information on equipment installation, including switch settings, power requirements, and general notes on cabling.

6. Module Logic Diagrams and Schematics - Shows the logic diagram and schematic of individual logic modules. Sometimes referred to as Module Data Sheets, when both diagram and schematic are together. These have not yet been collected together, re-drawn, and published as one book, therefore they must be ordered individually. Drawing #129931 contains all the appropriate drawing numbers or ordering these logic diagrams and/or schematics.

7. Product Design Specifications - Gives the design characteristics of a device. Frequently, when new equipment is being manufactured, the Product Design Spec is the only document listing pertinent hardware information. After a Reference and Technical Manual have been produced this document usually has only historical value.

8. Test Specifications - Shows the test procedure used by manufacturing test to bring up a piece of equipment, and sometimes contains useful information for the field.

9. Others - Engineering drawings are also produced which show assembly drawings, specifications, and other hardware and software related items which may be of use to you in the field. The eight documents listed above are felt to be the most important of these engineering drawings.

Diagnostics

Diagnostics are prepared by Diagnostic Programming and are distributed by the Publications Stockroom on receipt of an approved Literature Request Form (SDS 267).

Diagnostics consist of a Program Description (book form) and the diagnostic itself, prepared on either magnetic tape, paper tape, or punched cards. These two separate parts of a diagnostic are ordered individually under separate publication numbers.

The Program Descriptions usually contain a rather brief description of how the program operates, pointing out success or error indications, and a symbolic listing of the program. Some have included flow diagrams to help explain the program.

Diagnostics are currently undergoing changes and in the future should include much more information on how to use the diagnostics in troubleshooting equipment, rather than relegating them to being used only as a confidence tool.

The following page is a complete listing of all diagnostics available in the Sigma product line, showing the publication numbers for both the program and the manual (Program Description).

Development Division - Diagnostic Program Chart

Class	Device	Test	Σ7 Program	Σ7 Manual	Σ5 Program	Σ5 Manual	Σ2 Program	Σ2 Manual
CPU-I/O CHANNEL-OPTIONS: MEMORY		MEDIC	704067	900825	704067	900825	704022	900676
		INTERLEAVE	704121	901071	704121	901071		
		INTEG.	704447	XXXXXX	704447	XXXXXX		
		BOSO EXT.					704449	901514
		BOSO MINI					704962	901521
CPU-I/O CHANNEL-OPTIONS: CPU		SENSE	704041	900824			704008	901006
		VERIFY	704042	900870	704042	900870		
		PATTERN	704043	900891	704043	900891	704010	901015
		AUTO	704044	900872	704287	901523	704011	901007
		SUFFIX	704045	900893	704174	901519		
		FLOAT	704046	900898	704046	900898		
		DECIMAL	704047	900908				
		MAP	704048	900920				
		EDIT	704049	900897				
		INTERRUPT	704143	901134	704143	901134	704009	901016
		MEM PROTECT	704062	901516	704062	901516		
CPU-I/O CHANNEL-OPTIONS		RTC	704017	901136	704017	901136	704139	901164
		PFS	704122	901135	704122	901135	704140	901160
		MIOP	704057	901126	704057	901126		
		SIOP	704788	901158	704788	901158		
		IIOP			704018	901161	704006	901131
		EXT. INT.	704143	901134	704143	901134	704002	901137
		CPU-CPU INT.						
		I/O UTILITY					704000	901127
		FSC	704786	901193				
		CFE'S	704340	901535	704340	901535		
ASR	7020, 8092		704059	901133	704059	901133	704015	901163
			704069	901132	704069	901132	704024	901155
			704059	901133	704059	901133	704015	901163
			704069	901132	704069	901132	704024	901155
KSR	7010, 8091		704059	901133	704059	901133	704015	901163
			704059	901133	704059	901133	704015	901163
PAPER TAPE STATION	7060		704069	901132	704069	901132	704024	901155
LINE PRINTER	7440, 7440, 7445	UNMODIFIED	704063	901123	704063	901123	704019	901159
		MODIFIED	704777	901145	704777	901145	704019	901159
CARD DEVICES	7120, 7122, 7140, 7160	READ	704052	901125	704052	901125	704003	901162
		READ	704052	901125	704052	901125	704003	901162
		PUNCH	704052	901125	704052	901125	704003	901162
MAGNETIC TAPE UNITS	736X, 737X, 732X	7 CHANNEL	704026	901165	704026	901165	704051	901536
		9 CHANNEL	704066	901129	704066	901129	704021	901166
MAGNETIC DISC FILES	720X, 722X, 721X, 728X	MED. SPEED	704072	901130	704072	901130	704027	901167
		HI CAP	704978	901540	704978	901540	704980	901538
		HI SPEED	704979	901531	704979	901531		
		MASS STORAGE						
DISPLAY EQUIPMENT	753X, 7550	PLOTTER	704050	901518	704050	901518	704001	901517
		KB SCOPE	704004	901507	704004	901507	704012	901508
		CRT DISPLAY						
SYSTEM TEST		MONITOR	704138	901076	704138	901076	704700	900841
		LINE PRINTER	704349	901085	704349	901085	704707	901146
		KSR ASR	704350	901086	704350	901086	704706	901147
		RAD	704351	901090	704351	901090	704705	901148
		MT9	704352	901119	704352	901119	704701	901149
		CARD PUNCH	704353	901120	704353	901120	704703	901150
		CARD READER	704354	901121	704354	901121	704702	901151
		PAPER TAPE	704355	901122	704355	901122	704704	901152
DIAGNOSTIC CONTROL		DCP	704070	900712	704070	900712	704025	900839
		GEN. & SEL.					704030	901124
		BINARY	704356	900972	704356	900972	704361	901128
		RELOC. LOADER						
COMMUNICATIONS ORIENTED	760X, 7611, 7618	DSC	704013	901509	704013	901509	704055	901510
		COC	704016	901156	704016	901156	704014	901168
		AUTO DIAL	704074	901511	704074	901511	704156	901512
APPLICATIONS ORIENTED	77XX	PERIPH. SW	704314	901539	704314	901539		

For Internal Distribution Only

Development Division - Diagnostic Program Chart

CPU-I/O CHANNEL-OPTIONS — MEMORY / CPU

CLASS / DEVICE / COMPUTER	MEDIC	INTERLEAVE	INTEG.	8050 EXT. M.	8050 MINI-M.	SENSE	VERIFY	PATTERN	AUTO	SUFFIX	FLOAT	DECIMAL	MAP	EDIT	INTERRUPT	MEM PROTECT
Σ7 PROGRAM	704067	704121	704147	N	N	704041	704042	704043	704044	704045	704046	704047	704048	704049	704143	704062
Σ7 MANUAL	900825	901071	X	N	N	900824	900870	900891	900872	900893	900898	900908	900920	900897	901134	901516
Σ5 PROGRAM	704067	704121	704147	N	N		704042	704043	704287	704174	704046	N	N	N	704143	704062
Σ5 MANUAL	900825	901071	X	N	N		900870	900891	901523	901519	900898	N	N	N	901134	901516
Σ2 PROGRAM	704022	N	N	704449	704962	704008		704010	704011	N	N	N	N	N	704009	N
Σ2 MANUAL	900676	N	N	901541	901521	901006		901015	901007	N	N	N	N	N	901016	N

CPU-I/O CHANNEL-OPTIONS — OPTIONS

CLASS / DEVICE / COMPUTER	RTC	PFS	MIOP	SIOP	IIOP	EXT. INT.		I/O UTILITY	FSC	CFELS	MIOP-4BYTE
Σ7 PROGRAM	704017	704122	704057	704788	N	704143		N	704786	704340	705292
Σ7 MANUAL	901136	901135	901126	901158	N	901134		N	901193	901535	901554
Σ5 PROGRAM	704017	704122	704057	704788	704018	704143		N	N	704340	705292
Σ5 MANUAL	901136	901135	901126	901158	901161	901134		N	N	901535	901554
Σ2 PROGRAM	704139	704140	N	N	704006	704002		704000	N	N	N
Σ2 MANUAL	901164	901160	N	N	901131	901137		901127	N	N	N

ASR (7020, 8092) / KSR (7010, 8091) / PAPER TAPE STATION (7060) / LINE PRINTER (7440, 7440, 7445) / CARD DEVICES (7120, 7122, 7140, 7160, 7165)

CLASS / DEVICE / COMPUTER	ASR	ASR	ASR	ASR	KSR	KSR	PAPER TAPE STATION	LINE PRINTER UNMODIFIED	LINE PRINTER MODIFIED	CARD READ	CARD	CARD PUNCH	CARD LO-SPEED PUNCH
Σ7 PROGRAM	704059	704069	704059	704069	704059	704059	704069	704063	704077	704052	704052	704052	705290
Σ7 MANUAL	901133	901132	901133	901132	901133	901133	901132	901123	901145	901125	901125	901125	901552
Σ5 PROGRAM	704059	704069	704059	704069	704059	704059	704069	704063	704077	704052	704052	704052	705290
Σ5 MANUAL	901133	901132	901133	901132	901133	901133	901132	901123	901145	901125	901125	901125	901552
Σ2 PROGRAM	704015	704024	704015	704024	704015	704015	704024	704019	704019	704003	704003	704003	705291
Σ2 MANUAL	901163	901155	901163	901155	901163	901163	901155	901159	901159	901162	901162	901162	901553

MAGNETIC TAPE UNITS (736X, 737X, 732X) / MAGNETIC DISC FILES (720X, 722X, 721X, 728X) / DISPLAY EQUIPMENT (753X, 755X)

CLASS / DEVICE / COMPUTER	7 CHANNEL	9 CHANNEL	MED. SPEED	HI CAP	HI SPEED / MASS STORAGE	PLOTTER	KBD DISPLAY
Σ7 PROGRAM	704026	704066	704072	704978	704979	704050	704004
Σ7 MANUAL	901165	901129	901130	901540	901531	901518	901507
Σ5 PROGRAM	704026	704066	704072	704978	704979	704050	704004
Σ5 MANUAL	901165	901129	901130	901540	901531	901518	901507
Σ2 PROGRAM	704051	704021	704027	704980	N	704001	704012
Σ2 MANUAL	901536	901166	901167	901538	N	901517	901508

SYSTEM TEST / DIAGNOSTIC CONTROL & LOADERS / COMMUNICATIONS ORIENTED (7601, 7611, 7618, 7650) / APPLICATIONS ORIENTED (77XX, 7670)

CLASS / DEVICE / COMPUTER	MONITOR	LINE PRINTER	KSR	ASR	RAD	MT 9	CARD READER	CARD PUNCH	PAPER TAPE / LO-SPEED PUNCH	DCP	GEN. & SEL.	BINARY LOADER	RELOC. LOADER	EX. SYMBOL	DSC	COC	AUTO DIAL	CIU	PERPH. SW	DCT-2000
Σ7 PROGRAM	704138	704349	704350	704351	704352	704353	704354	704355	705301	704070			704356	N	704013	704016	704074	705279	704314	704983
Σ7 MANUAL	901076	901085	901086	901090	901119	901120	901121	901122	901564	900712			900972	N	901509	901156	901511	901551	901539	901550
Σ5 PROGRAM	704138	704349	704350	704351	704352	704353	704354	704355	705301	704070			704356	N	704013	704016	704074	705279	704314	704983
Σ5 MANUAL	901076	901085	901086	901090	901119	901120	901121	901122	901564	900712			900972	N	901509	901156	901511	901551	901539	901550
Σ2 PROGRAM	704700	704707	704706	704705	704701	704703	704702	704704	705302	704025		704030	704361	705299	704055	704014	704156	705297	705296	705298
Σ2 MANUAL	900841	901146	901147	901148	901149	901150	901151	901152	901563	900839		901124	901128	901558	901510	901168	901512	901560	901549	901559

Rev. C 10/1/68 LEGEND: X-NOT PUBLISHED AS MANUAL N-NOT APPLICABLE

Installation Documents

Installation Documents are prepared by Marketing Operations and are distributed as part of the "Site Documentation" which accompanies all equipment shipped to a specific installation site. These documents are used to install a specific installation and contain only information unique to that installation. These documents consist of:

1. Installation Instruction/Control Sheet (IICS)
2. Installation Material List (IML)
3. Computer Assembly Chart (CAC)
4. Installation Cable List (ICL)
5. Installation Floor Plan (IFP)
6. Installation Cable Chart (ICC)
7. Installation Power Chart (IPC)
8. Configuration Diagram (CD)

Some installations may not require all of these eight documents, however, most installations will have at least the first 4 documents.

The following pages contain sample sheets of the various documents listed above, along with explanatory information when needed.

Installation Instruction/Control Sheet

This sheet is used primarilly to show the status of the other parts of the Installation documents, and to provide a place for Marketing Operations to inform the installers of deviations in installation which have precedence over more "standard" installation practices, or deviations in shipping, or other important information necessary to insure that the installation is performed correctly.

Headings

CUSTOMER - Names the customer receiving the equipment

PRODUCT LIST REF - Refers to the Product List or Sales Order number.

INSTALLATION NO. - The number assigned to this specific installation and no other.

SHOP ORDER NO. - Internal use only; no significance for installation purposes.

INSTRUCTIONS - This area is used when Marketing has important information to transmit to thos installing the equipment. This area should always be read when installation is started.

REVISIONS - Shows revision status of the Instructions.

REVISION STATUS - Lists the individual revisions of the remaining documents.

SDS

INSTALLATION INSTRUCTION / CONTROL SHEET

CUSTOMER

PRODUCT LIST REF

INSTALLATION NO.	REV.
SHOP ORDER NO.	
APPROVALS	DATE
	SHEET

INSTRUCTIONS

REVISIONS

REVISION STATUS

II CS					IML										CAC					ICL																					IFP									
A 1	A 2	A 3	A 4	A 5	B 1	B 2	B 3	B 4	B 5	B 6	B 7	B 8	B 9	B 10	C 1	C 2	C 3	C 4	C 5	D 1	D 2	D 3	D 4	D 5	D 6	D 7	D 8	D 9	D 10	D 11	D 12	D 13	D 14	D 15	D 16	D 17	D 18	D 19	D 20	E 1	E 2	E 3	E 4	E 5					

Installation Material List

This sheet or sheets are used to list, by model and assembly number, all equipment to be installed.

Headings

CUSTOMER - Name of the customer receiving the equipment

C.S. CODE NO. - Not used

SALES ORDER REF. - The Sales Order (SO) number; may be one or many.

INSTALLATION NO. - The number of this unique installation.

SHOP ORDER NO. - Internal use only; not significant for installation purposes.

S.O. REF. - The Sales Order for the equipment appearing on that line.

S.O. NO. - Sequence number starting with 1.

S.O. QTY. - Number of units of the type appearing on this line.

MODEL NUMBER - The Model Number of the unit appearing on this line.

DESCRIPTION - A brief description of the unit, such as "CPU".

M.L. NO. - Sequential numbers for reference

ASSEMBLY NUMBER - The manufacturing assembly number of the unit.

ASSEMBLY CHART - Refers to the Computer Assembly Chart (CAC) which appears on one of the other documents.

NO. - The page number of the CAC

LOCATION - Shows Frame and Row (chassis) in which the unit is installed.

UNIT QTY. - Number of units actually shipped.

PULL QTY. - Not Used

QTY. ISSUE - Not Used

QTY. B.O. - Not Used

SOURCE - Indicates the source of the equipment:

"M" = Manufacturing
"D" = Development Engineering
"F" = Field
"S" = Systems
"P" = Refurbishment or Stores

WEEK REQ. - An alpha character A-Z which refers to a Shipping Group (if applicable) listed on the IICS, where there may be a deviation of shipment.

SHIP WEEK - Internal use only; no significance for installation.

SERIAL NO. - Not Used

REV. IND. - Revision Indicator; indicates that a revision has been made to a line, but does not reflect the number of changes.

SDS

INSTALLATION MATERIAL LIST

INSTALLATION NO. | REV.

CUSTOMER | C. S. CODE NO. | SHOP ORDER NO. | REV.

SALES ORDER REF. | APPROVALS: | DATE: | SHEET OF

S.O. REF.	S.O. NO.	S.O. QTY.	MODEL NUMBER	DESCRIPTION	M.L. NO.	ASSEMBLY NUMBER	ASSEMBLY CHART NO.	ASSEMBLY CHART LOCATION	UNIT QTY.	PULL QTY.	QTY. ISSUE	QTY. B.O.	Source	WEEK REQ.	SHIP WEEK	SERIAL NO.	REV. IND.

1261 (8/67)

Computer Assembly Chart

The CAC is used to determine the physicall placement of the various cabinets that make up a system, excluding the placement of peripheral equipment. The cabinets are broken down into the various frames, where the prefix F = Front, C = Center, and R = Rear frame. In older and current CAC's, each row (numbered 1-9) contains a number which corresponds to the M.L. NO. in the Installation Material List (IML). In newer versions of the CAC, each row will have the model number of the unit to installed (or is installed) in that row and frame.

SDS

SIGMA 7 AND SIGMA 5

COMPUTER ASSEMBLY CHART

INSTALLATION NO.	REV.
SHOP ORDER NO.	REV.
APPROVALS:	DATE: SHEET

F29	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0	F15	F16	F17	F18	F19	F20	F30
1																		1
2																		2
3																		3
4																		4
5																		5
6																		6
7																		7
8																		8
9																		9

C29	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0	C15	C16	C17	C18	C19	C20	C30
1																		1
2																		2
3																		3
4																		4
5																		5
6																		6
7																		7
8																		8
9																		9

R29	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	R15	R16	R17	R18	R19	R20	R30
1																		1
2																		2
3																		3
4																		4
5																		5
6																		6
7																		7
8																		8
9																		9

EQUIPMENT VIEWED THRU FRONT

Installation Cable List

Probably the most important of all the documents, the ICL shows the exact routing off all cables supplied with the system which are not already installed, and also those which were left installed when the equipment was shipped.

Headings

C/L NO. - Cable List Number; a sequential numbering of all cables for reference. This number does not appear on the cables themselves.

ASSY NO. - The manufacturing assembly number of the cable.

BASE - the basic assembly number of the cable.

LNTH - Length of the cable, where the first two digits are tenths of feet, and the last digit is a times ten multiplier:

101 = 1 Ft. ($.10 \times 10^1$)

102 = 10 Ft., etc.

MASTER ID NO. - Not Used

MODEL NO. - Redundant information relating to the CAC. Ignore.

DESCRIPTION - Brief description of the cable function, such as "Power Monitor #1", or "Priority Cable".

FROM/TO - indicates the beginning and end of all cables:

FRM - Frame, as designated by the CAC; examples:

F7	Front Frame, Cabinet 7
C7	Center Frame, Cabinet 7
R7	Rear Frame, Cabinet 7
PD	Power Distribution Panel
BR4	Bottom, Rear of Cabinet 4
BF4	Bottom, Front of Cabinet 4
SC,FSC	Free Standing Console
KP1	Keyboard Printer #1
PT1	Paper Tape Station #1
CR1	Card Reader #1
CP1	Card Punch #1
LP1	Line Printer #1
GP1	Graph Plotter #1

CHS - Chassis (row), numbered 1-9 from top to bottom.

CONN - Connector (module location), numbered 1-32.

E/C - Cable is connected to the etch side (E) or component side (C) of module.

T/B - Terminator/Blank on cable;

T	Standard Terminator (127315)
Ⓣ	Priority Terminator (128047)
B	Blank Terminator (115832)
TX, BX, ⓉX	Remove Terminator already installed

ROUTE VIA - Indicates how the cable should be routed:

B	Bottom
BF	Bottom Front
BR	Bottom Rear
DIR	Direct
EXT	External
HS	Higned Side
INT	Internal
LS	Latched Side
T	Top
TF	Top Front
TR	Top Rear

REV - Revision status, showing changes in a line.

SDS

INSTALLATION CABLE LIST

INSTALLATION NO.		REV
CUSTOMER		
APPROVALS	DATE SHEET	

C/L NO.	ASSY NO. BASE	ASSY NO. LNTH	MASTER ID NO.	MODEL NO. FROM	MODEL NO. TO	DESCRIPTION	FROM FRM	FROM CHS	FROM CONN	FROM E/C	FROM T/B	ROUTE VIA	TO FRM	TO CHS	TO CONN	TO E/C	TO T/B	REV

1341 (1-67)

Installation Floor Plan

The IFP is only a recommended floor plan supplied to the customer by Marketing Operations, depending upon the customer's desires. When supplied, it is a scale drawing showing the actual dimensions of the various cabinets, their placement in regards to the site location, and where power (unspecified here) needs to be brought to. When supplied, the IFP will also be the basis for establishing cable lengths.

The power call-outs are usually symbolic, and provide a reference to the Installation Power Chart (IPC).

SDS

INSTALLATION FLOOR PLAN

INSTALLATION NO.	REV.
CUSTOMER	
APPROVALS.	DATE: SHEET OF

Installation Cable Chart

The ICC, when provided, is a diagram generated from the ICL, showing, in diagram form, the cable runs. This chart is not important for installation, and is seldom used.

SDS

INSTALLATION CABLE CHART

INSTALLATION NO.	REV.
CUSTOMER	
APPROVALS	DATE
	SHEET OF

Installation Power Chart

The installation power chart is used more in the installation planning stage than in actual installation. It indicates all power required by the site, and the amount of 2Khz power required by the various frames.

Headings

KEY - Symbolic reference to the Installation Floor Plan, which refers to the primary power required (customer provided).

MODEL NUMBER - The circuit which the primary power feeds. Such as, PT14/PT15, PT19, MPD, etc.

BAY/FRAME - The Cabinet and Frame, which relates to the next column on the right.

2.0KHZ SDS REF. - The computed 2Khz power (output of PT15) required by each Frame; expressed in percentage of 1 PT14/PT15 output.

LINE POWER IN VA, RECEPTACLE, and BREAKER - all refer to the primary power connections listed under KEY.

BTU/hr. - Relates to the number of BTU's for each PT14/PT15/MPD combination.

SDS

INSTALLATION POWER CHART

INSTALLATION NO.	REV.
CUSTOMER	
APPROVALS	DATE SHEET

KEY	MODEL NUMBER	BAY FRAME	2.0KHZ SDS REF.	CUSTOMER PROVIDED			BTU/Hr.
				LINE POWER IN VA	RECEPTACLE	BREAKER	
			TOTAL VA			TOTAL BTU	

Configuration Diagram

The Configuration Diagram is another redundant document which is rarely used. It provides a simple block diagram of all the installed units with lines connecting them together to show functional relationships.

SDS

CONFIGURATION DIAGRAM

INSTALLATION NO.		REV.
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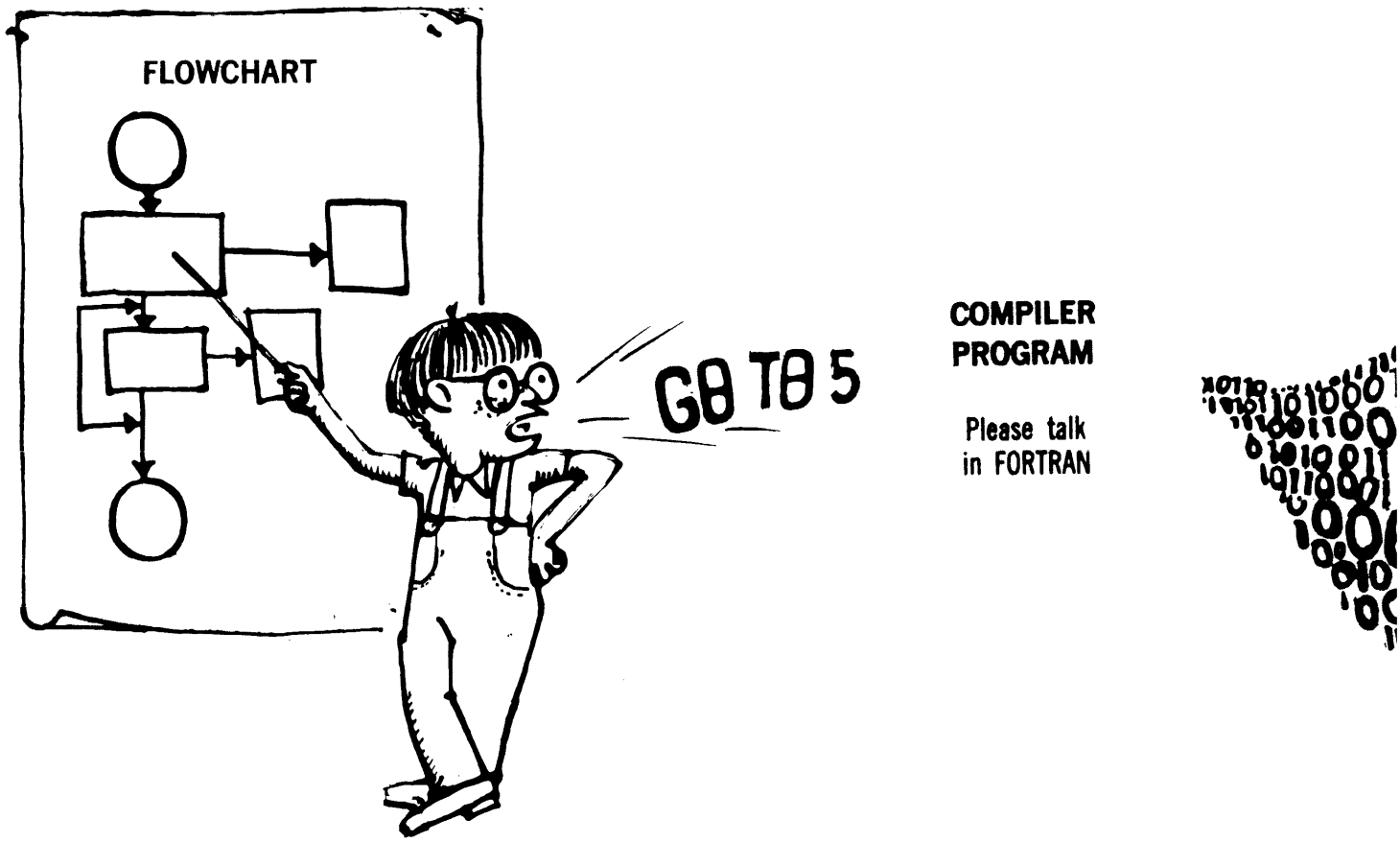
SOFTWARE PRIMER

SECTION VII

A SOFTWARE PRIMER

R.J. SPINRAD, SDS
VICE PRESIDENT, PROGRAMMING



A software primer for

by ROBERT J. SPINRAD, *Brookhaven National Laboratory, Upton, New York*

When a researcher goes shopping for a digital computer he needs to have quite specific objectives in mind. If he goes out for bids on a computer without having thought out very carefully what it is he really wants, he will soon find himself buffeted about by the very confusing claims, counterclaims and new ideas thrown at him by the various computer manufacturers.

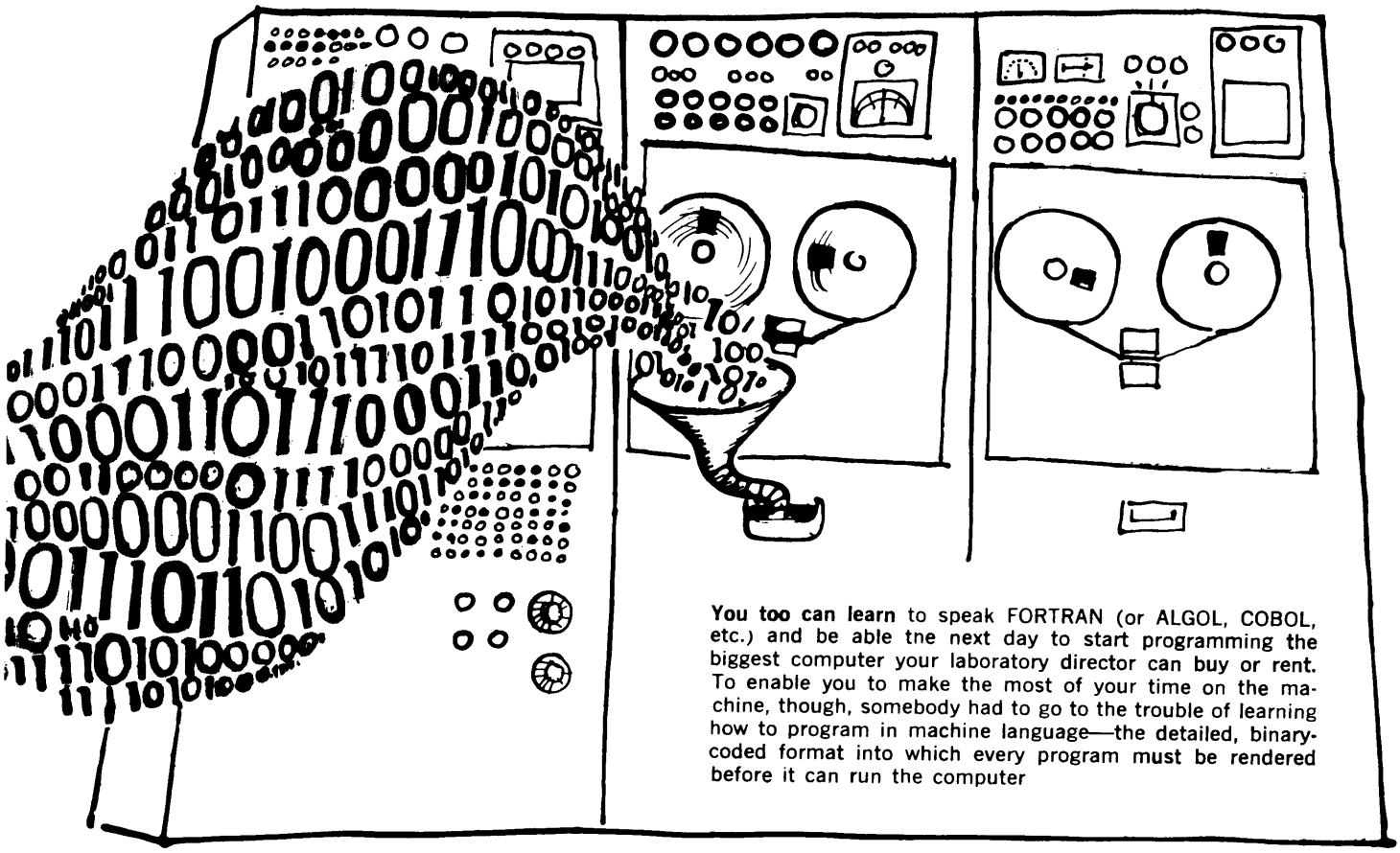
One of the things he has got to understand from the first is that the crates of hardware the manufacturer will deliver to his door do not constitute a computer system—the *hardware* provides only the potential for the system he envisions. To realize that system, he has to assemble the appropriate *software*—the set of computer programs that will enable his collection of hardware components to carry out the operations he has in mind. Not only should he have some idea of what a computer program is but he must have a clear understanding before he invests in any hardware just where the software he needs is going to come from. How much can he expect to get from the manufacturer on magnetic tape free-of-charge? How much of the programming is he going to have to do himself or hire someone to do for him? This is only the beginning of the list of questions he must be able to ask himself about the software requirements, key to best use of machine.

Suppose we begin with the fundamentals and ask what is a computer program? The only real program is the "machine language" program. This is because computers don't "understand" FORTRAN or ALGOL or Swahili. The only "message" to which the digital computer will make an electronic response is the message contained in the string of binary digits comprising the instruction word.

Thus, the only programs that operate in the most sophisticated modern computers are binary —or machine language—programs. The most complex reactor code, the most recondite chess playing program functionally must exist in the computer's memory as a list of binary instructions.

In the very early days of computing the only way to construct a program was to write it directly in the binary form. Even today there are occasions when the programmer must have recourse to this most primitive of techniques. Programming in this way is, by modern standards, excruciatingly tedious, unproductive and error-prone.

It took a few years for computer scientists to understand how they could "bootstrap" them-



You too can learn to speak FORTRAN (or ALGOL, COBOL, etc.) and be able tne next day to start programming the biggest computer your laboratory director can buy or rent. To enable you to make the most of your time on the machine, though, somebody had to go to the trouble of learning how to program in machine language—the detailed, binary-coded format into which every program must be rendered before it can run the computer

aspiring computer owners

selves out of the dilemma caused by the fact that the computer's language was not a comfortable one for man. The solution, in retrospect, seems obvious: Write a program (in machine language) that will be able to translate a human-compatible language into the machine-compatible one. This insight and the developments that have evolved from it are among the most fundamental to the computer revolution.

PROGRAMS THAT PRODUCE PROGRAMS

The first programs-to-produce-programs were symbolic assemblers. An assembler is a program which is able to convert any other program written in symbolic-assembler language into the directly equivalent machine-language version.

Symbolic-assembler language differs from binary machine language in many ways that ease the programmer's task. Most important is that the symbolic assembler language allows the programmer to express his program in terms of alphabetic symbols and decimal numbers. The conventions (syntax) of the symbolic language free the programmer from virtually all the tedious binary manipulations which so characterize machine-language programming.

Assemblers do, however, still require the programmer to construct one symbolic instruction for each binary instruction in the translated program. (The input, "higher level" language program is called the "source" program. The output program, produced by the translator, is called the "object" program. For the simple examples we are discussing here, the object programs are binary, machine-language programs.) While such "one-to-one" assemblers are quite adequate for many tasks—and essential for some—sophisticated programmers soon developed the need for still "higher level" languages.

Macro-assemblers. The next higher level of source language is the macro-assembler language. (All these terms are generic. Each existing translating program and its source language has its own name such as MAP or MACRO.) Generally speaking, macro-assemblers allow the user to construct frequently needed subprograms or procedures in such a way that they can be called or specified in the body of the program by using

ROBERT J. SPINRAD, head of the Computer Systems Group at Brookhaven, was one of the pioneers in the design of computer systems to be used on-line with experiments in basic research.

only a single program word. Thus a single line of source language code can invoke a detailed and complex subprogram.

This is a significant improvement over the simple one-to-one assembler technique. Although superficially appearing to be little more than an extra-convenient assembler, the macro-assembler is, in fact, qualitatively different and must be viewed as intermediate between an assembler and a compiler (discussed below).

The progression from binary to assembler to macro-assembler represents more than just an increasing sophistication and convenience of programming language. Paralleling the language development there is the important contrapuntal theme of program organization. At each stage there is apparent a greater segmentation and structuring of the program parts. The macro-assembly programmer is encouraged by the character of the programming language to modularize his program's trigonometric computations, its input-output operations, its sorting functions. The availability of modularized, "building-block" subroutines from the computer manufacturer or the community of users encourages this kind of organization.

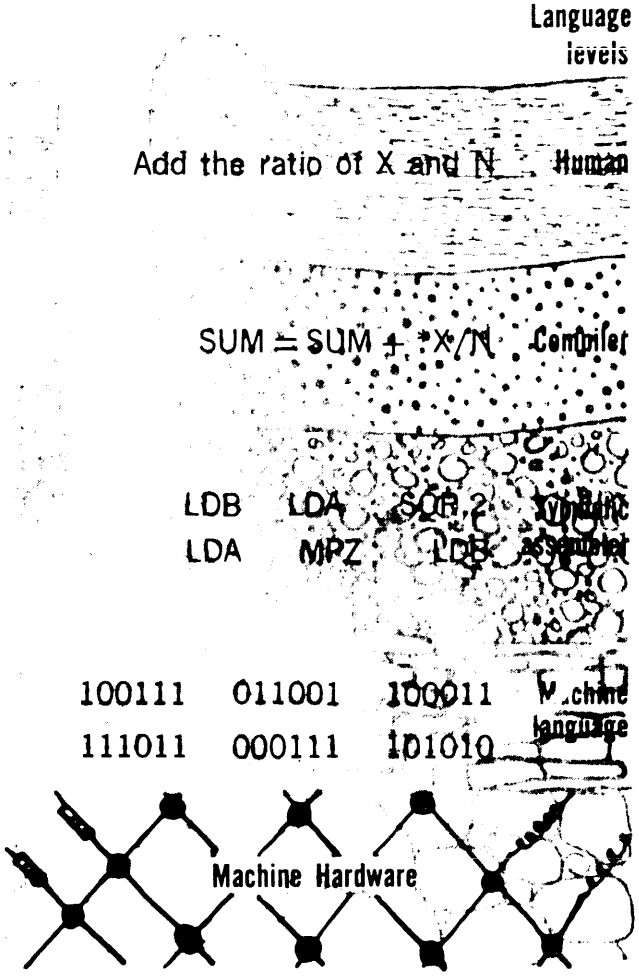
Thus the programmer finds more and more that he is using portions of programs (pieces of "software") that he did not write himself. From here it is a small step to the concept of the compiler.

Compilers. With compilers, the idea of one-to-one source language to machine language translation is abandoned entirely. Compilers are task-oriented rather than computer-oriented. (In fact, machine-independence is a frequent object of the compiler designer.)

The most commonly used compilers are FORTRAN and ALGOL. FORTRAN was originally designed for FORmula TRANslation, though its applicability has been much broadened since. ALGOL, standing for ALGOrithmic Language, is most popular in Europe and is used as a language of interchange by computer specialists. Hundreds of compilers and compiler languages exist. Each one is tailored to a particular problem class (e.g. COBOL—COmmon Business Oriented Language).

Since compiler languages are designed to relate to people and not to machines there is, in general, a most complex relationship between the source program and the object program. In fact, compiler-level programmers do not even need to know the machine language to construct, test, and run their programs. This significant simplification has opened up the world of the computer to the bulk of today's users.

It is important to realize, however, that some of the features of higher level languages that make them most attractive are exactly the ones that make them inappropriate for situations in which the programmer needs to exploit every detailed advantage of speed or performance the computer can afford him. Thus programs whose operation represents a large fraction of the computer's total utilization are often "polished" at the machine language or symbolic level. For instance in a matrix inversion program a frequently recurring routine (or inner loop) would be calculating the sums of products of matrix elements. One could reduce the running time by locating the part of the FORTRAN program that relates to these calculations and rewriting it in machine language.



Hierarchy of languages between man and machine. Originally everyone had to program in machine language. Higher level languages were invented to make programming easier

Similarly, programs that interact with external equipment are almost invariably written at the symbolic level because they present very difficult problems of timing and efficiency. For instance, a program that handles the transfer of information between the core memory and a disc-storage device must be written in machine language.

Recognizing this need, many of the newer versions of existing compilers allow the intermixing of compiler-level and symbolic-level coding in the user's program. These extensions to the compiler's syntax allow free, symbolic cross referencing of problem variables between the two language levels.

From the point of view of organization and structure, the compiler-produced program represents the maturity of the concepts of modularity and independently produced subprograms. At the binary level, the programmer needing, say, a Sine

routine would have to either create it himself or painfully transliterate it. At the symbolic and macro-symbolic levels the Sine program would be available in general (relocatable) form and could be incorporated into the user's program with ease. (It would be easier in the macro-assembler because of facilities for external referencing.) The programmer would, nevertheless be responsible for physically obtaining and inserting the Sine routine into his program. At the compiler level, the programmer need only write the word "SINE" and leave it to the compiler to obtain, incorporate, and link it to his program.

Thus when one buys a computer today that "has" FORTRAN, say, the magnetic tapes on which the manufacturer provides the FORTRAN program will contain a set of machine-language subroutines for the simpler functions such as trigonometric functions, logarithmic functions, etc. The manufacturer can usually provide certain other subroutines not included in this basic FORTRAN package along with simple directions for incorporating them into the compiler.

More specialized routines, for instance a particular matrix inversion procedure, might not be available as machine-language subroutines. But often the user can obtain from users' groups or other contacts a routine written in some compatible language which he can then incorporate into his program.

Another kind of software of interest to someone buying a computer is the availability of routines to help in debugging programs—locating errors in newly written programs when the user first tries them out on his machine. A number of the manufacturers provide software which greatly facilitates debugging and more and more this is becoming part of the package which the manufacturer supplies. When one solicits bids it is wise to ask for a "debug" package to be included.

PROGRAMS THAT RUN PROGRAMS

Up to this point we have discussed situations in which only one program operates at a time. Machine-language programs whether produced by hand, by assemblers, or by compilers may be loaded into the computer, started, and run to completion. The compiler or assembler is itself a program. It is loaded, accepts input data (the source program), produces output data (the object program), and then stops.

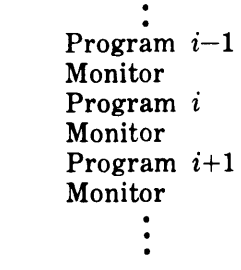
The critical element in these operations is that a single task runs to completion. The task (program) may be simple or complex. The important point is that it does not have subtasks which may be stopped or started in arbitrary and uncorrelated ways. Wherever the situation demands the overlapped operation of programs, fundamental changes in the mode of computer operation are required. The most important of these changes is that a "monitor program"—a program to run programs—is necessary. A monitor may be required for a variety of reasons.

Batch processing. Probably the easiest to understand in principle—though the details may be staggeringly complex—is the use of a monitor program for batch processing. "Batch processing" is, simply, the running, one after the other, of a series of independent programs, each one being completed before the next one is initiated.

However, as we have been discussing this mode of operation, there was always understood to be a person—the programmer, an operator—who took each program, loaded it, started it, removed it when completed, and then went on to the next program. This is, in fact, the way that the earliest computer centers worked.

It requires no extraordinary insight, however, to see that the human can be replaced by a program— a batch monitor program. The monitor's functions are identical to those of the human operator that it replaces. It is responsible for running programs taken from an input queue and printing, punching, or writing the results, one after the other, on some sort of output medium.

Let us examine the important change in operating principle that this implies. In batch processing under monitor control there are always two programs simultaneously in residence in the core memory of the computer—the monitor program and a user's program. They do not operate simultaneously; a single computer can be running only one program at any instant of time. Rather they alternate with this pattern:



The monitor program is, in a sense, never completed, except when the computer is turned off for the day. The monitor's task is to consistently perform the necessary "red tape" functions incident to the operation of the succession of user's programs.

Most important, there exists a definite hierarchy in rank. The monitor is the superior program. It "owns" the computer and merely "lends" it to the succession of user programs. The monitor program is permitted the use of all the resources of the computer and its ancillary equip-

ment. User programs are restricted. For example, a user program does not have the right to issue a HALT command to the computer. Rather, at the completion of its task, it must yield or transfer control to the monitor. Similarly, most of today's sophisticated monitor programs do not allow the user program the privilege of operating the input-output equipment. When one of these functions is to be performed, the user program must request the monitor to do it.

Monitor programs become more and more complex as they are called upon to handle multiple processors and multi-level storage devices.

Time-sharing. "Time-sharing" is a very confusing term because it has been used to describe so many different things. One can be sure however—in no matter which of its incarnations it appears—that it implies some sort of monitor in an operating system.

Before we go on, however, let us outline some of these inter-related terms:

- *"Multiprogramming"* is generally used to describe the overlapped operation of two or more user programs.
- *"Real-Time"* operations, whether multi- or single-programmed, are operations in which the computer system is responding to, and keeping pace with, the demands of some external device.
- *"Time-sharing"* operations then involve both multiprogramming and real-time operations.

Thus, a configuration comprised of two teletypes answering questions for two operators and working through a single computer would be a "real-time, time-shared, multiprogrammed operating system."

Returning to the exposition, we can see that a multiprogramming operating system may be considered a monitor system with more than one user program in the computer at one time. This means that, in addition to loading and unloading user programs, the multiprogramming or time-sharing monitor must adjudicate among them in regard to the allocation of system resources for which there are simultaneous demands.

Sometimes this is handled by the very simple technique of giving each program a "turn" at the computer for a fixed-time slice in "round-robin" fashion. More often the allocation algorithm is a very complex one—taking into account such things as job priorities, request "aging," and efficiencies of equipment utilization.

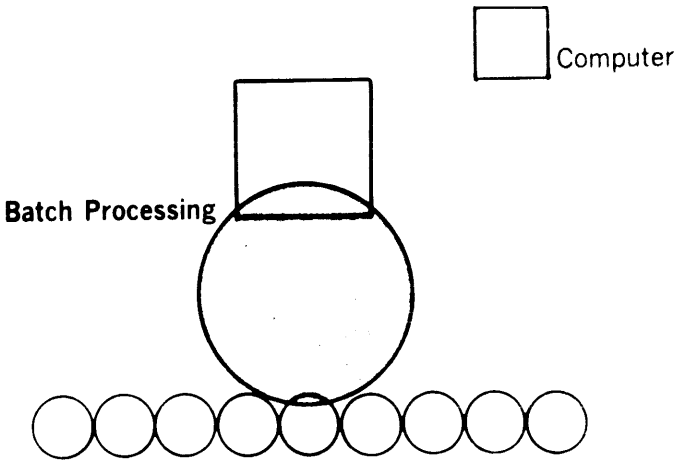
What kind of monitor programs are available to some one who buys a computer these days? Here the situation is much more muddied than for the compiler programs. Almost all of the manufacturers of small and large computers claim that they provide monitor systems.

The problem is that the term "monitor system" is not as precise a term as FORTRAN compiler or COBOL compiler. The user has to outline in much greater detail what it is he expects of the system before he can sensibly question the manufacturer.

For a simple monitor system the man who wants to take a chance and who wants to educate himself can, with a couple of months of hard work, learn enough to make an intelligent choice. However, the same man with the best of intentions cannot in a couple of months understand enough about the intricacies and complexities of any sizeable operating system to make a choice by himself. This is best left to the expert.

COMPLEX SYSTEMS

An example of the complexities that one runs into for even medium-sized systems is the need continually to transfer or swap information between the core memory and a fast auxiliary memory. So far we may have given the impression that the computer's core memory held, permanently, all the current user's programs, the monitor, the compiler, the input/output programs, and the loader and other service routines. This is not the case. The core memory is the most expensive part of the machine and lots of core costs lots of money.



HOW MONITOR PROGRAM FUNCTIONS FOR

To keep the core-memory size to a minimum the overwhelming majority of modern operating systems are "swapping systems." That is, they are systems in which the currently nonactive programs are "swapped" (transferred) to an external drum or disc memory. The reasons for this are entirely financial: Drum and disc memories are one to three orders of magnitude less expensive, per word, than core memories. It is poor design not to take advantage of the economies of external storage.

Of course, the system designer pays the penalty of decreased performance when he employs an external store. External memory of this type cannot provide either rapid or simple access to a single datum. Rather, data or programs must be transferred in large blocks between the core memory and the rotating memory. These trans-

fers take time and the information cannot be used until it is resident in the core memory.

Much of the skill in designing an effective swapping operating system lies in structuring it so that these constraints exact the least penalty in non-productive "overhead" time. The designer must be master of both hardware and software techniques. The "systems" interaction is felt here more than in most other areas.

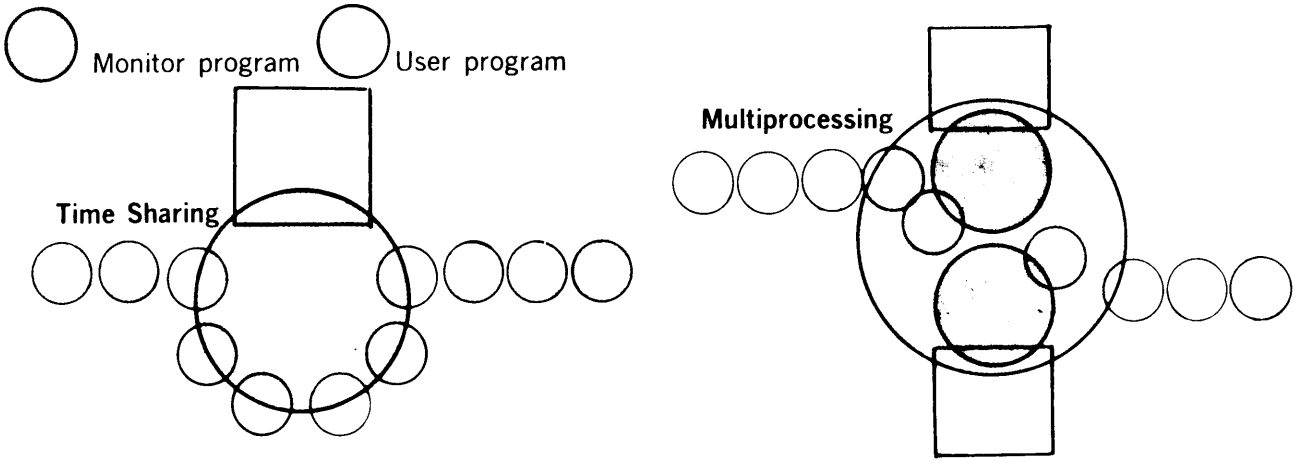
Most computer systems of medium size and up employ swapping. Even when there are real-time system tasks which require microsecond response —and thus cannot be swapped—other, less demanding portions, may employ swapping.

Multiprocessor systems. There is still another aspect of the software picture that we must touch upon: multiprocessor systems.

Multiprocessing should not be confused with multiprogramming. Recall that multiprogramming was described as more than one program in a single processor (computer). Multiprocessing exists when one or more programs are operating in more than one processor.

The term multiprocessing is, as many of these others are, very broad. The auxiliary computers can range all the way from fairly simple input/output processors to duplicates of the main processor. There can be many or only a few processors working in concert in a multiprocessor system. The purposes of multiprocessor configurations are varied. We list some of them here:

- *Increased computational power.* This is an obvious one. The design objective—unfortunately not always realized—is to have the coupled processors provide more service than they would if operated independently.
- *Task matching.* It is often appropriate to have a simple (inexpensive) computer handle simple tasks that would waste the power of the main computer. The relegating of input/output operations, or file management, or operator communications, to an auxiliary computer is a good example of this application of multiprocessing.
- *Safety.* When properly organized, multiple processor configurations can exhibit a "fail-soft" property. That is, when one of the processors fails, the whole system does not stop but rather suffers only a degradation in performance. Such systems are costly and are found mostly in industrial process control or in military situations.
- *Functional separation.* Sometimes it is reasonable to assign the separate portions of the system to separate processors. The supervisory monitor might go into one, the real-time tasks into another, and the batch processing might take place in a third. This category often overlaps with task matching.



DIFFERENT MODES OF COMPUTER OPERATION

Almost all of the types of operating systems described in preceding sections can be, and are, run in multiprocessor configurations. For the most part, the same system design criteria obtain.

Mixed systems. More and more these days one encounters claims from manufacturers that their computer—and operating system—will be "all things to all people." What lies behind these claims?

Because the computer is such a wondrous engine there is probably some substance to all that is said. It is certainly possible to design a computer system that will take experimental data, run scientific computations, operate remote terminals, monitor the fire alarm system, and perform the organization's business accounting on the side.

The important question is whether it is sensible to design such a system. Most multipurpose systems are soundly conceived and soundly executed. But it is important to realize that not every combination of functions that springs to the mind of man is appropriate to a single computer system. It is all too easy to fall into the trap that goes something like this: "As long as we have the computer here, we might just as well let it handle (function *X*)." *Beware!*

POWER MONITOR AND POWER SUPPLIES

SECTION VIII

Sigma Power Monitor

3-5202 The Sigma 7 optional power fail-safe feature monitors the primary power sources and provides automatic shutdown in cases of partial or complete power failure where power drops below given limits. If power returns to an acceptable level, normal operation resumes automatically. During power fail-safe shutdown, information in certain volatile flip-flop registers is stored in core memory to prevent critical program data loss. When power is restored, the information in core memory is returned to the volatile flip-flop registers so that the program can resume at or near the interrupted point. Core memory serves as the storage device during power fail-safe operation since the cores are nonvolatile and retain information without the presence of power.

3-5203 The power fail-safe feature is composed of two major components: the power fail-safe interrupts, which initiate the save and recovery programs, and the power monitor assembly, which monitors the primary power source.

3-5204 INTERRUPTS

3-5205 When a power failure occurs, the power fail-safe feature notifies the CPU by means of a power-off interrupt. Sufficient energy is stored in the Sigma 7 power supply system to maintain dc power for the duration of a short power failure subroutine. When primary power resumes, a power-on interrupt causes the CPU to enter a recovery subroutine that restores the CPU to the state existing before the lapse of power.

3-5206 The interrupt memory locations are X'50' for the power-on interrupt and X'51' for the power-off interrupt. The power-on interrupt is the highest priority interrupt in the system; power-off interrupt has second highest priority. Both of these interrupt levels are always enabled; they cannot be disarmed, disabled, inhibited, or triggered under program control.

3-5207 Power Monitor Assembly - General

3-5208 Figure 3-640 is a simplified block diagram of the power monitor assembly, a standard equipment item in Sigma 7, which consists of three standard modules: (1) the WT21 regulator and independent power supply, (2) the WT22 line detector, and (3) the AT13 line driver.

3-5209 The WT21 regulator is used to supply regulated dc voltages to the WT22 line detector and AT13 line driver.

3-5210 The WT22 line detector performs the function of detecting a power failure and indirectly providing the necessary signals to the CPU for a start-up or shutdown sequence.

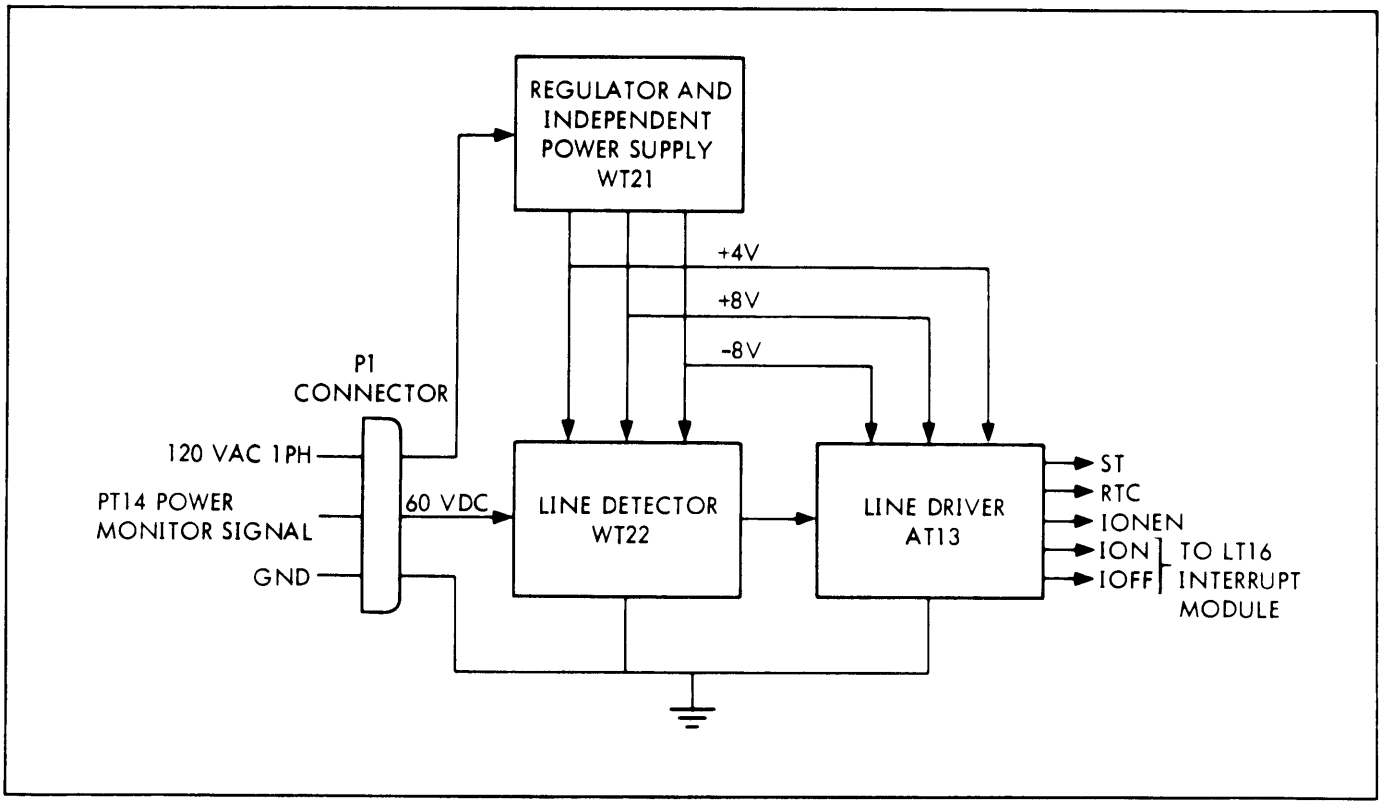


Figure 3-640. Power Fail-Safe Feature, Simplified Block Diagram

3-5211 The AT13 line driver is basically a cable driver used to drive the output signals of the WT22.

3-5212 Although the primary power sources are optional, depending on user requirements, the primary power source shown in the simplified block diagram is single phase 120 vac.

3-5213 The application of primary power to the Sigma 7 system power supplies provides the power fail-safe feature with the voltage necessary to power the WT21, WT22, and AT13 modules. These standard dc voltages are provided by the internal power supply in the WT21 regulator. The power fail-safe feature receives 120 vac and 60 vdc power when primary power is applied. The 120 vac power is transmitted to the WT21 regulator, which in turn is converted to regulated +4 vdc, +8 vdc, and -8 vdc. The regulated dc voltages are transmitted to the WT22 and AT13.

3-5214 The 60-vdc power output from the PT14 power supply is monitored directly to the WT22 line detector, which senses this input and the other dc voltages to determine whether they are within acceptable limits.

3-5215 The requirements for a start-up or shutdown sequence are governed by the WT22 line detector, which contains the basic sensing circuits within the power fail-safe feature. Detection of one or more out-of-tolerance voltages by the WT22 line detector will generate the necessary logic signals to the AT13 line driver for a fail-safe shutdown. A subsequent return of voltages that are within tolerance will generate the necessary logic signals to the AT13 line driver for a fail-safe start-up.

3-5216 Real-Time Clock. The real-time clock circuit on the WT22 module generates a stable clock frequency synchronized to the line frequency. This real-time clock is not an integral part of the power fail-safe feature and is located on the WT22 primarily for purposes of convenience.

3-5217 Input Requirements. NOTE: The input power source will vary according to user requirements. For information on the various power sources, refer to the section on Power Distribution.

3-5218 Three-Phase Input Detection. When three-phase operation is used, one phase is used to supply power to the power monitor. The presence of three phases is detected by sensing the presence of a three-phase rectified but unfiltered 60-vdc signal supplied by the PT-14 power supply.

3-5219 Single-Phase Detection. Single-phase detection is provided for by a simple rewiring in the power monitor. When rewired, this standard 110-vac line is the only external input to the power monitor assembly.

3-5220 Internal Power Supply. The power monitor has its own internal power supply capable of delivering power to the WT21, WT22, and AT13 modules. This supply comes into operation when external power is applied. When power is shut off this internal supply outlasts the dc supplies in the computer, thereby keeping logic signals in their appropriate state as power decays and the power-off subroutine is executed.

3-5221 Parallel Operation. The power monitor is capable of paralleling its output with the output of other power monitors. This is necessary, since several power monitors may be used to monitor individual lines and power supplies in a system. Therefore, if more than one power monitor is used in a given installation, the equivalent logic outputs of the power monitors are ORed together.

3-5222 Output Signals. There are five output signals from the AT13 line driver: (1) ST, the master reset signal, (2) ION, which initiates the start-up sequence, (3) IOFF, which initiates the shutdown sequence, (4) IONEN, the ION enable signal, which performs an AND function for the output of the power monitor assembly, and (5) RTC, the real-time clock signal, which is a clock synchronized to the line frequency, but is not used directly in the power fail-safe feature.

3-5223 Power Monitor Assembly - Circuit Description

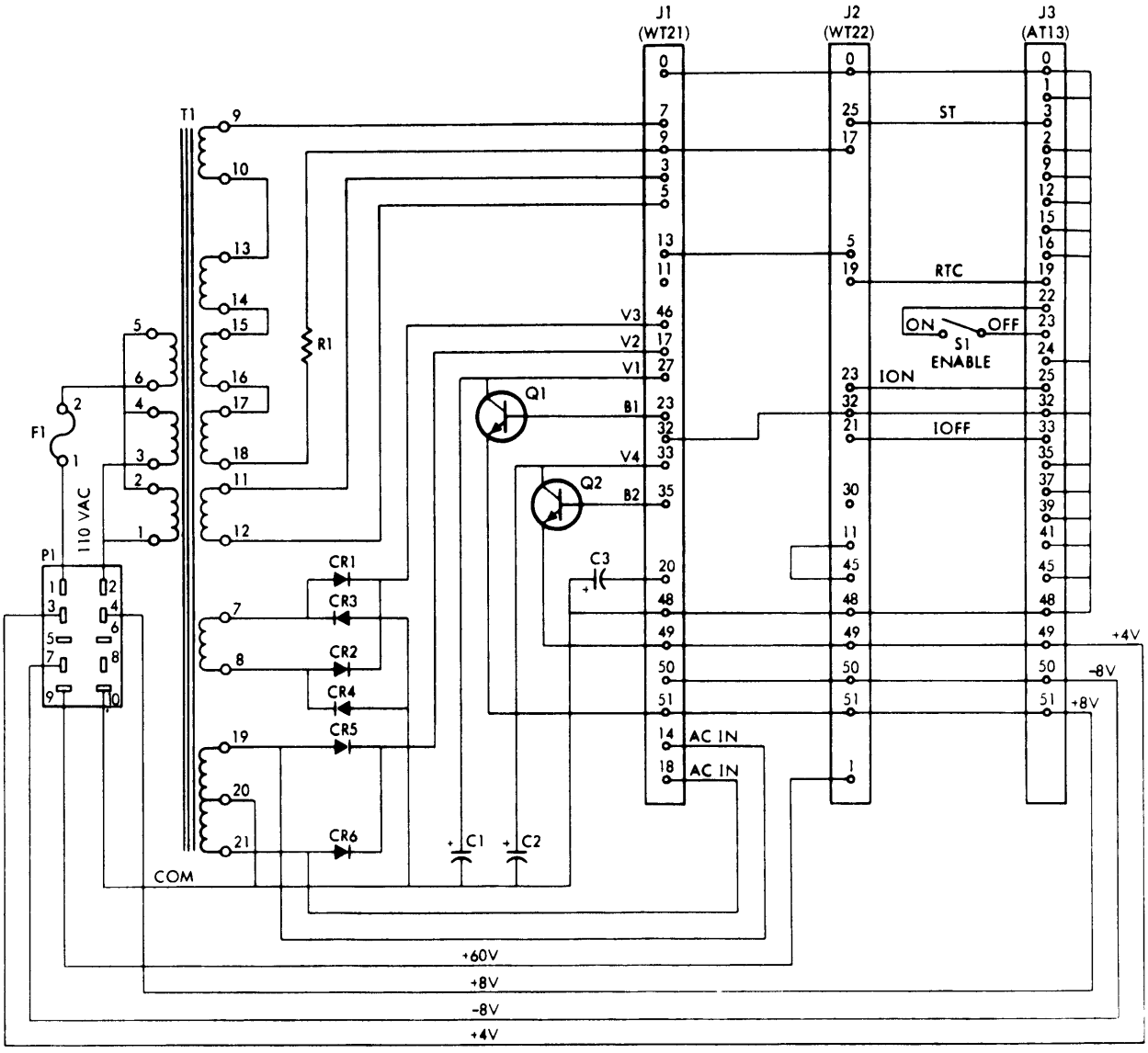
3-5224 Figure 3-641 is a functional schematic of the power monitor assembly. Input power to the internal power supply on the WT21 regulator is shown to be single phase 110/120 vac from pins 1 and 2 of the P1 connector. This input power is transmitted to transformer T1, which is in the internal power supply of the WT21 regulator package. Diodes CR1 through CR4 comprise a full-wave bridge rectifier and provide the dc inputs to the +8 vdc and +4 vdc regulator drivers. Diodes CR5 and CR6 act as a full wave rectifier providing ac input to -8 vdc regulator circuit.

3-5225 WT21 Regulator

3-5226 The WT21 (see figure 3-642 for schematic) is the voltage regulator-driver used to supply regulated dc to the WT22 power monitor. The WT21 contains a +8 vdc regulator-driver, +4 vdc regulator-driver, and -8 vdc regulator. The +8 volt and +4 volt drivers are used with external pass transistors. The -8 volt regulator contains the pass transistor located on the module. The -8 volt regulator contains a rectifier circuit to allow operation from ac inputs at pins 14 and 18. The +8 and +4 volt regulator-drivers require dc input voltages. Two additional bridge rectifying circuits are located on the WT21 to provide 24 vdc and 50 vdc.

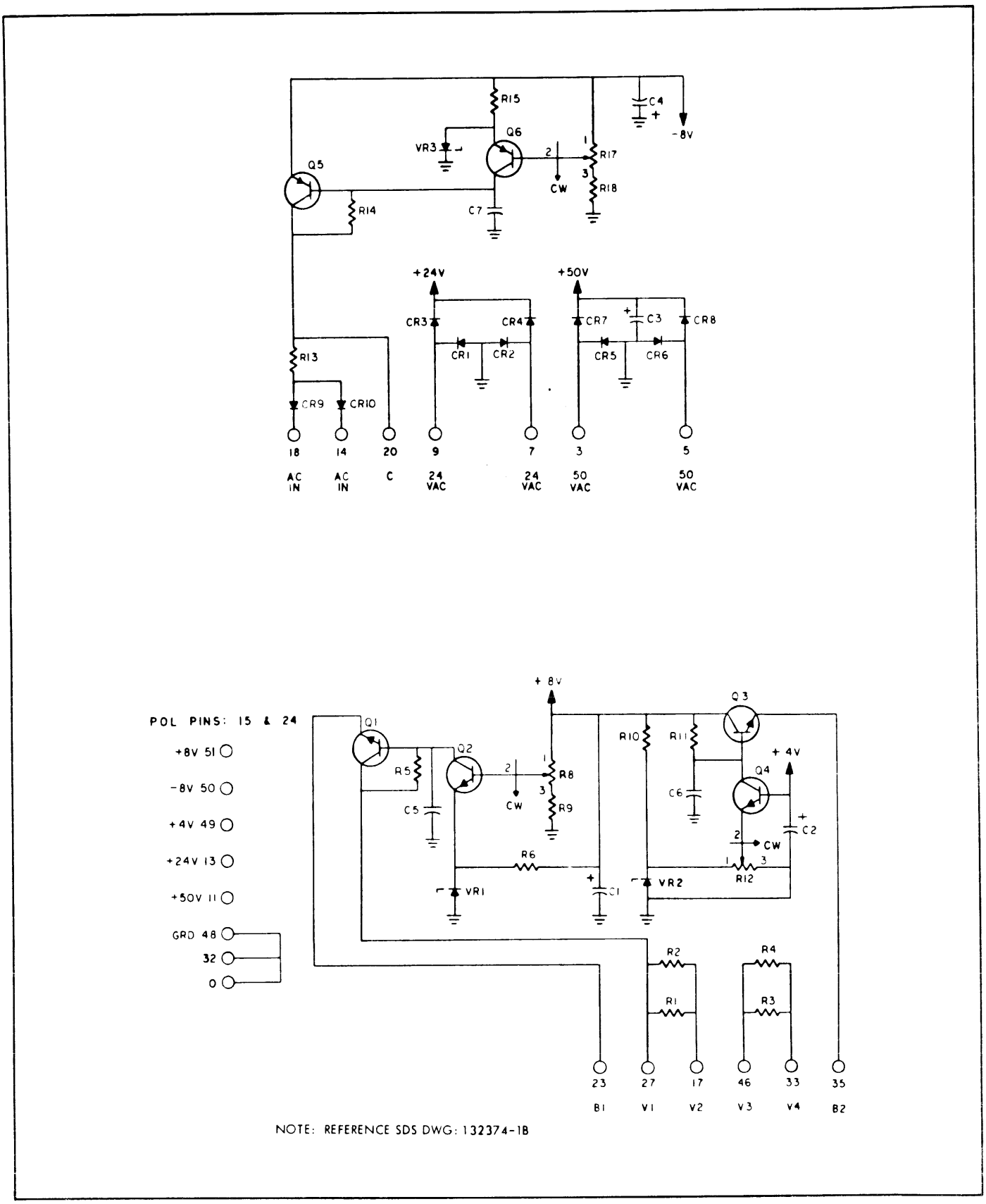
3-5227 Filter capacitors for input filtering to the series regulators are not located on the module; however, provisions are made for external connections. Surge resistors are located on the WT21 to prevent damage to the external rectifiers that supply current to the +8 vdc and +4 vdc regulators.

3-5228 R1 through R4 are the surge protection resistors. CR1 through CR4 and CR5 through CR8 rectify the ac input



NOTE: REFERENCE SDS DWG: 132391-1B

Figure 3-641. Power Monitor, Functional Schematic



NOTE: REFERENCE SDS DWG: 132374-1B

Figure 3-642. WT21 Regulator, Schematic

voltages, which are then used to operate the power monitor with 24 vdc and 50 vdc.

3-5229 +8 VDC Regulator. Q2 and Q1 are the sense and drive transistors used in the +8 vdc regulator. The input of the regulator is pin 17 (V2). Pin 27 (V1) is brought out to connect to an external filter capacitor. Voltage adjustment is accomplished by controlling the current in Q2. This current is determined by the emitter voltage, which is the reference voltage, and the sampled base voltage as adjusted by R8. The Q1 emitter output drives the external pass transistor.

3-5230 +4 VDC Regulator. Q3 and Q4 are the drive and sense transistors for the +4 volt regulator. Collector voltages to Q3 is derived from the +8 volt supply. Drive voltage to Q3 also comes from the +8 volts, therefore providing preregulation for the +4 volt regulator. Q3 drives a power transistor external to the WT21. The base of Q4 is connected to the +4 volt output. Current is controlled by changing the reference voltage, R12, at the emitter of Q4.

3-5231 -8 VDC Regulator. The -8 volt regulator, including pass transistor Q5, is located on the WT21. CR9 and CR10 provide a negative supply voltage when ac is applied to pins 18 and 14. Pin 20 is the common and external capacitor connection. R17 provides voltage control of the output.

3-5232 WT22 Line Detector

3-5233 Figure 3-643 is a block diagram of the WT22, figure 3-644 is the WT22 schematic, and figure 3-645 shows the WT22 waveforms. Basic timing and input power for the WT22 are as follows:

Delay time D:	adjustable from 5 to 20 ms
ION time A:	300 ms ±10%
Power failure detection time:	< 3 ms
Input power:	+8 vdc @ 40 ma
	+4 vdc @ 30 ma
	+60 vdc @ 50 ma for 3Ø detection
	+22 vdc @ 10 ma for 1Ø detection

3-5234 The WT22 is the line detector module that provides all output signals for the power monitor. This is the basic unit within the power fail-safe feature. The principal function of the WT22 is to detect a power failure and provide the necessary reset and interrupt signals for the CPU. These signals provide start-up and shutdown sequences when power comes on and goes off.

3-5235 Start-up Sequence (See figure 3-644). When power is first turned on, the 307 flip-flop is dc set by V1 (+8 vdc), charging C8, causing ST to go high. VD, the ION threshold voltage, is also applied and will charge C4 through R13. The voltage across C4 is determined by the magnitude of VD through R13, as well as the time constant R13-C4. This time constant will determine the time after power has been turned on that the threshold sensing circuit will trigger the ION pulse. As shown in figure 3-645, the occurrence of ION is time A, or the time necessary for all dc power supplies in the computer to stabilize. The ION pulse resets the 307 flip-flop and ST falls to 0. If ST is 0, the reset of the 307 flip-flop is high and prevents C4 from charging by holding the NOR gate on.

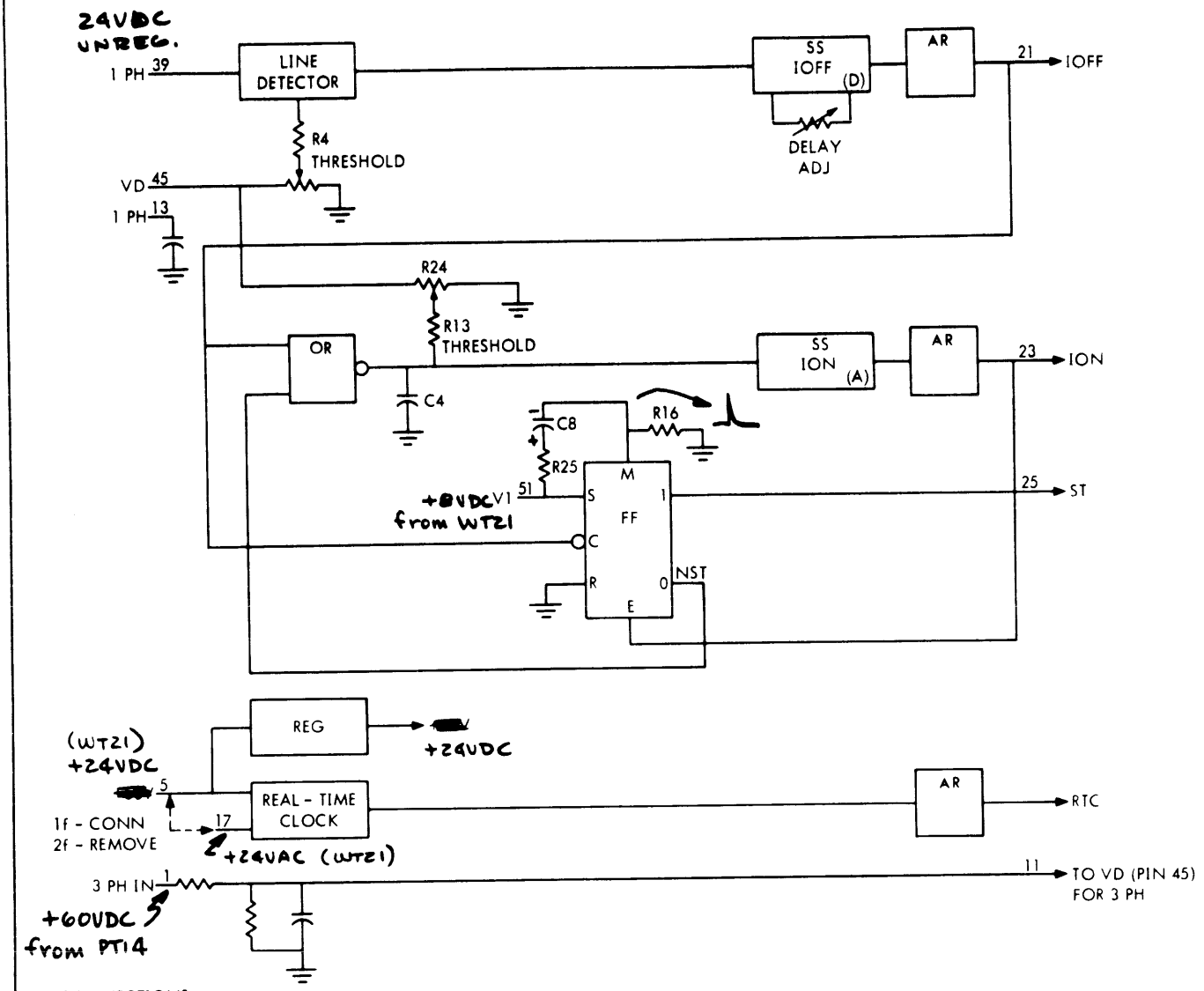
3-5236 Shutdown Sequence. When the line detection circuit indicates power failing it generates the IOFF signal. At the same time, the IOFF signal is delayed by the period D shown in figure 3-645. D is the maximum time dc power supplies will remain within regulation after a power failure. IOFF is applied to the clock input of the 307 flip-flop and since the set is held high, the flip-flop sets when IOFF returns to 0, which is at the conclusion of period D. IOFF pulses will continue to be generated as long as power is below the acceptable threshold level.

3-5237 IOFF pulses and NST prevent C4 from charging in case of a short power interrupt, as shown in figure 3-645. As long as IOFF produces a pulse, C4 will discharge, preventing an ION pulse until C4 charges up again. During this time ST is held high by IOFF, setting the 307 flip-flop continuously.

3-5238 ST will go false when ION goes true and there are no IOFF pulses present. This means that any time an IOFF pulse occurs, the entire start-up sequence will take place. When power returns, the line detection circuit will generate IOFF pulses whenever the line voltage drops below threshold. Threshold oscillation is prevented by a preset hysteresis. IOFF and ION, as determined by their respective threshold settings, may be set 10 volts apart; for example, IOFF will be present at 80 volts line and ION will occur at 90 volts line. ST will go high when the line drops below 80 volts and will remain high until the line raises above 90 volts.

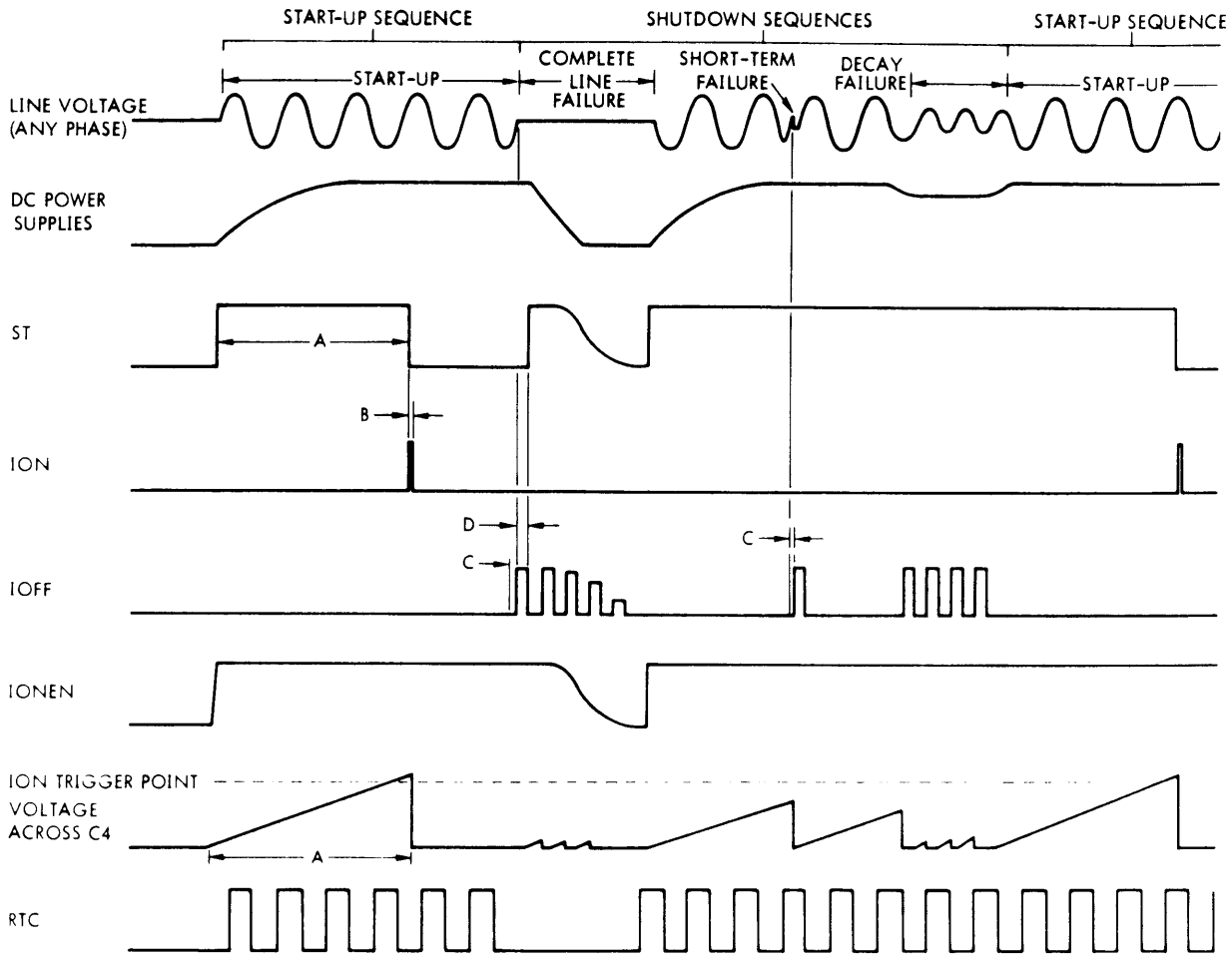
3-5239 Real-Time Clock Signal (RTC). In addition to the ST, ION and IOFF signals, the WT22 generates a real-time clock pulse (RTC) synchronized to the line frequency. By selecting the 1F or 2F term on the module this pulse will be at the line frequency or twice the line frequency.

3-5240 WT22 Power Supply. The WT22 is supplied with power by the internal power supply in the power monitor. A schematic of this power supply and its relationship to all the modules in the power monitor assembly is shown in figure 3-641.



CONNECTIONS :
1 PH - 24V UNREG TO 13 AND 45; CONN 5 TO 39 ; 1 AND 11 NO CONN
3 PH = INPUT TO 1; CONN 11 TO 45; 13 AND 39 NO CONN

Figure 3-643. WT22 Line Detector, Block Diagram



LEGEND

A. INITIAL TIME FOR DC SUPPLIES TO STABILIZE IS APPROXIMATELY 300 MS
B. 5-100 μSEC AFTER ST FALLS
C. RESPONSE OF IOFF AFTER COMPLETE LINE FAILURE - 1.0 MS
D. TIME BETWEEN IOFF AND ST OR MAXIMUM TIME POWER SUPPLIES WILL REMAIN WITHIN SPECIFICATIONS AFTER A POWER FAILURE IS 5 TO 20 MS

Figure 3-645. Power Fail-Safe Waveforms

3-5241 WT22 Line Detection Circuit Description

3-5242 The line detection circuit circuit is that part of the WT22 module which detects an ac line failure. The detection scheme is slightly different for single-phase and three-phase operation; however, both phases are detected by the WT22.

3-5243 Single-Phase Operation. Single phase operation is shown in figure 3-646. C1 cannot charge to level Vp if an ac signal is present at Ein, the single-phase input. Ein is generated by an unfiltered dc signal that is clamped to provide a steep rise at the zero crossing. This rise time determines the minimum response time of the IOFF pulse. C1 must charge to Vp, and Vp is determined by setting potentiometer R2. The time constant of R3C1 is longer than T1 as the voltage charges to Vp. In addition, the base voltage, VD, is derived from an unregulated source so it will decrease with line voltage, causing Vp to be at a lower point, Vp = n VBB where n is 0.7 and Vp is the firing point of the unijunction transistor Q2. If power drops out completely, Q2 will fire at less than one-quarter of a cycle, as set by R2. If power goes down slowly below threshold, Q2 will fire at a worst-case condition of one-half cycle caused by the decrease in VBB; however, this is only if power drops slowly below threshold and is not a worst-case condition. This happens because in this case the power supplies will take longer to come out of regulation.

3-5244 Three-Phase Operation. For three-phase operation the threshold is set below the crest of the multiphase signal, as shown in figure 3-647. This unfiltered signal supplies the VBB source voltage in three-phase operation. If any phase falls below threshold the unijunction transistor will trigger. Since the voltage is now sampled at six times the line frequency, response time will be faster than

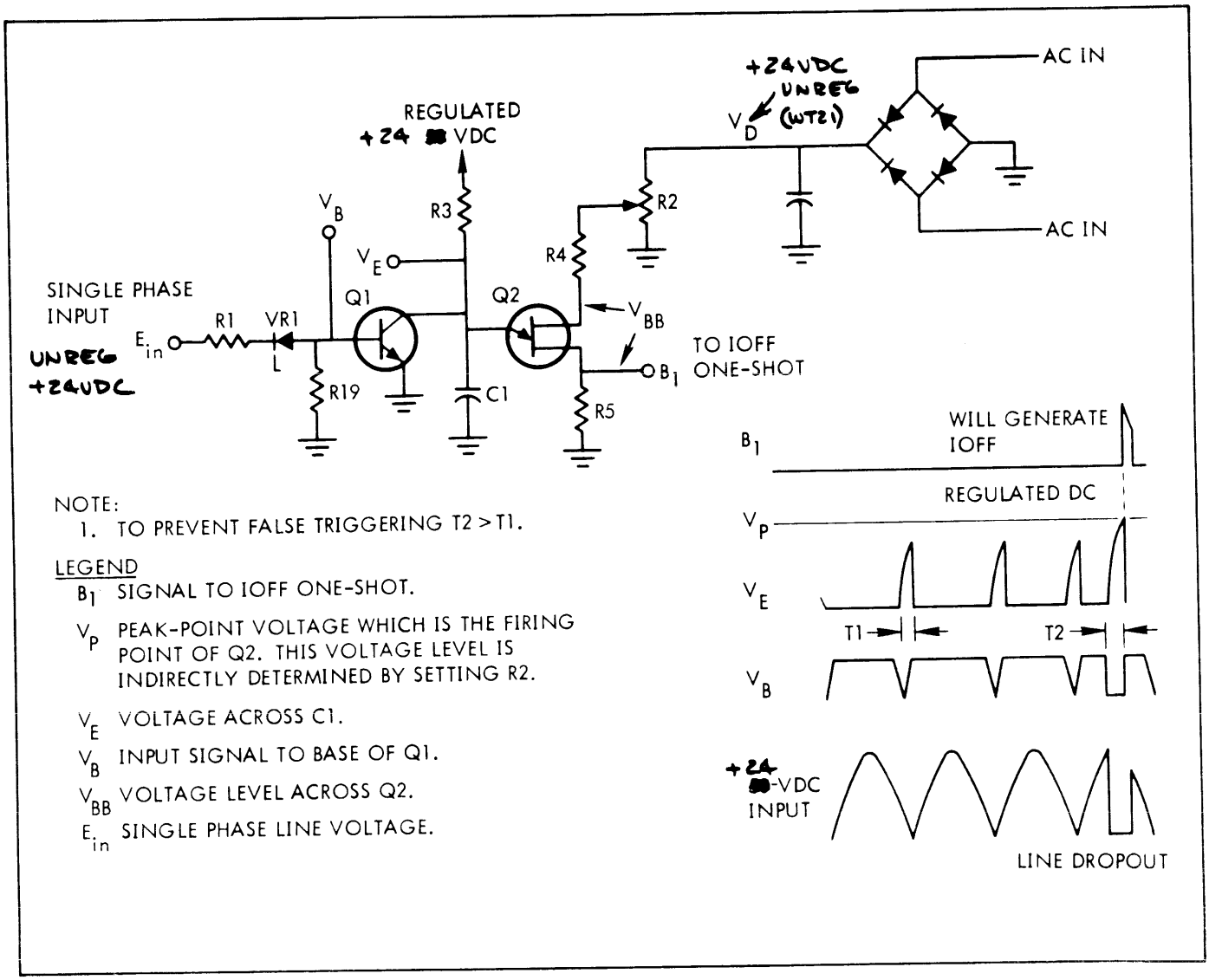


Figure 3-646. Single-Phase Detection

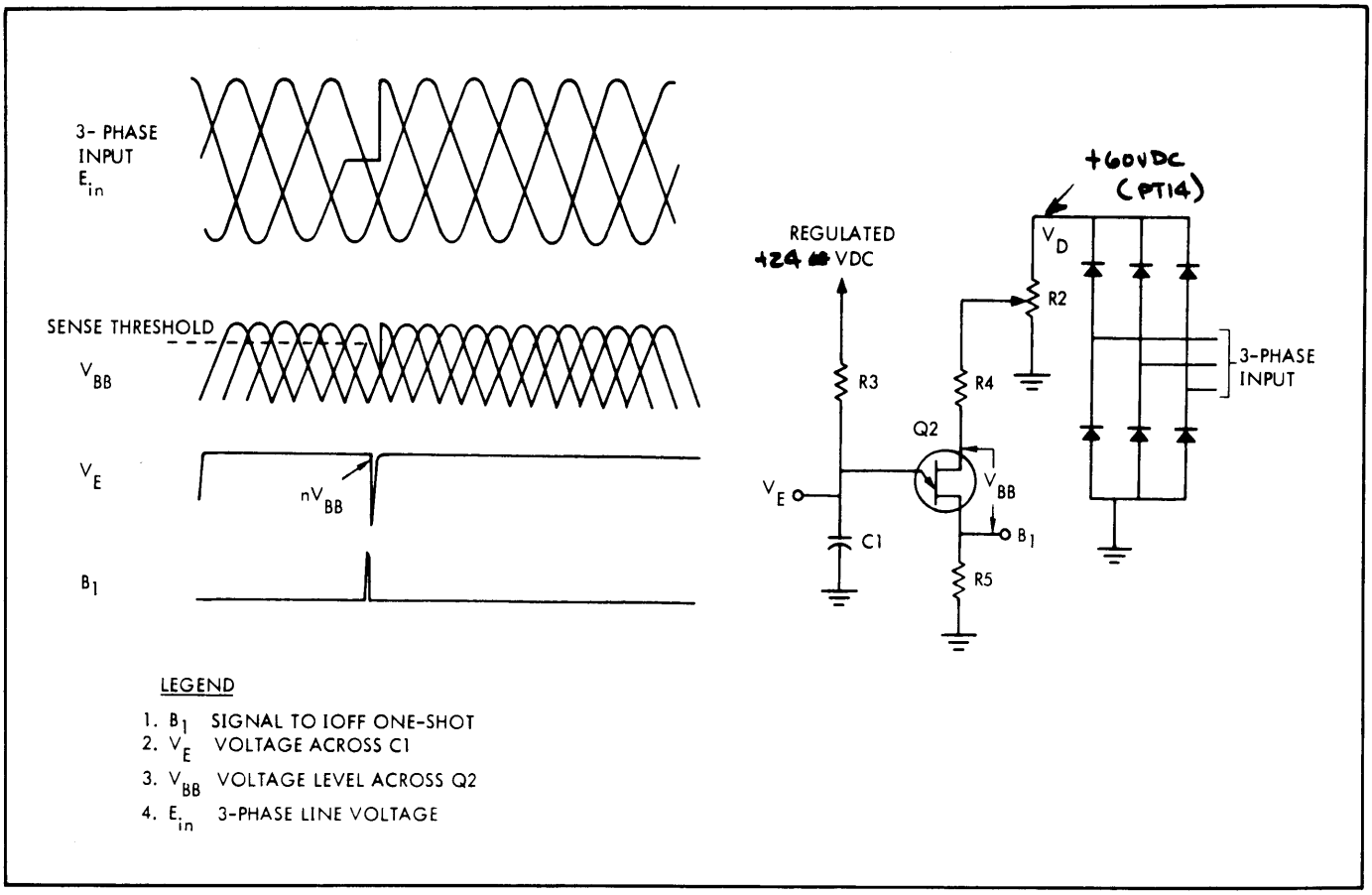


Figure 3-647. Three-Phase Detection

in single-phase operation. The additional transistor across C1 is not used and is therefore disconnected in three-phase operation by selection of the proper input connections to the WT22 module.

3-5245 Pin Connections. For single-phase operation, pin 39 is connected to pin 5 and 22 vdc is applied to pins 13 and 45. For three-phase operation, 60 vdc unfiltered three-phase is applied to pin 1, and pin 11 is connected to pin 45.

3-5246 ION One-Shot Operation. The ION one-shot is used to generate the ION pulse. This occurs when there are no IOFF pulses and the 307 flip-flop is in reset state with ST low if the line is above the ION threshold. The one-shot, shown in figure 3-648, consists of a unijunction transistor threshold circuit, an inverter, and a 2-input OR gate. If pulses are applied to D, the emitter voltages will never reach Vp on Q6; likewise, if R is positive Q5 will conduct and C4 will never charge. This provides the inhibit function of the one-shot. C4 will only charge if power is on and no IOFF pulses are present, which is the start-up routine. When Q6 fires it produces a pulse across R15 that is used to generate ION.

3-5247 Real-Time Clock Operation. The real-time clock will put out pulses at the line frequency or twice the line frequency, as shown in figure 3-649. Q7 derives its inter-base voltage VBB from a clamped high voltage unfiltered dc source. R20C7 is set to be longer than one cycle. As C7 is charged, VBB will suddenly be reduced, and Q7 will fire when Vp = n VBB and produce a pulse at B1. If single frequency pulses are required, Q7 must not fire every half cycle. C7 is prevented from charging by diverting the current through R20 through CR1 every other cycle.

3-5248 Power Monitor Logic

3-5249 There are five power monitor logic signals put out by the AT13 logic module. The signals and their cable pins are as follows:

Signal	Cable Pin
ST	04
RTC	07
IONEN	08
ION	09
IOFF	10

3-5250 The ION and IOFF signals are input to the LT16 interrupt module as shown in figure 3-650.

3-5251 Start-up Routine. The following steps outline the logic signals that make up the power monitor assembly startup routine.

a. ST is the master reset signal that is true during the time when power on-off transitions are occurring.

When power is applied this signal comes true as soon as possible (determined by the internal power supply). ST will remain high initially as the power supplies in the computer stabilize. This time is determined by ION occurring.

b. ION occurs only if the line voltage is above a preset level, which is the ION threshold. ION is then generated approximately 300 ms after power is turned on. When ION occurs, ST falls to 0. ION should outlast ST by more than 2 μsec but less than 100 μsec.

c. IONEN is a true signal as long as a power monitor is operating. This signal is necessary only when using more than one power monitor per system. It is available on an AT13 cable driver-receiver where the receivers and drivers are connected externally. This signal from a driver of one power monitor connects to the receiver of another, thus cascading the signals. IONEN then becomes an AND function which will only be true if all power monitors are operative.

3-5252 As shown in figure 3-641, the IONEN switch S1, is left open if only one power monitor is used in a system. If more than one is used, the IONEN switches are closed on all power monitors except the last switch in the cable scheme. This will be the IONEN switch closest to the cable terminator, and it is always left open. With S1 open, the IONEN signal will be high as long as primary power is applied to the power monitor. IONEN is ANDed with ION to produce the PON signal for the LT16 interrupt module so that the power-on interrupt subroutine can be initiated.

3-5253 RTC (Real-Time Clock). A clock pulse that is jitter-free and synchronized to the line frequency is one of the outputs. This output is arranged so that one RTC signal will not be paralleled with other RTC signals by the interconnecting cables. One of the isolated receiver-drivers on the AT13 is used for this purpose. This precaution is necessary since these RTC signals may be on different phases of the line.

3-5254 Shutdown Routine. The following steps outline the logic signals that make up the power monitor assembly shutdown routine.

a. IOFF is a signal that sets an interrupt channel indicating to the CPU that the line voltage is below a preset threshold. This interrupt initiates a shutdown subroutine that stores all volatile data into core storage before the master reset signal, ST, causes a cessation of memory operations. The IOFF pulse should be greater than 2 μsec, but less than 20 ms. The delay between a power failure and the IOFF pulse going true should be minimized (less than 2 ms for single phase, less than 1 ms for three phase).

b. ST will go true, after a delay time, when power fails. This delay time is determined by the amount of time it takes for the external dc supplies in the computer to fall below their specified tolerances. This delay time or the time between IOFF occurring and ST going true should be adjusted to as long a duration as possible to allow maximum time to store data before shutting down the input to the memory. The delay is adjustable between 5 to 20 ms.

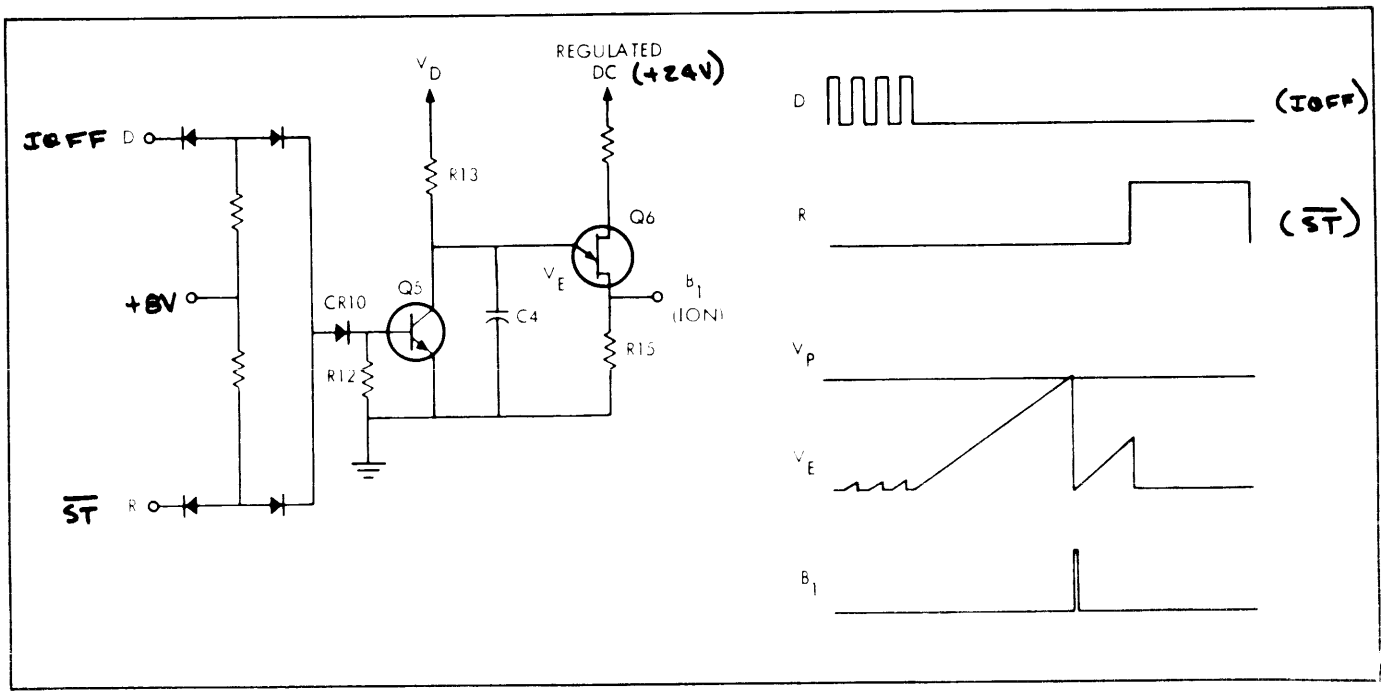
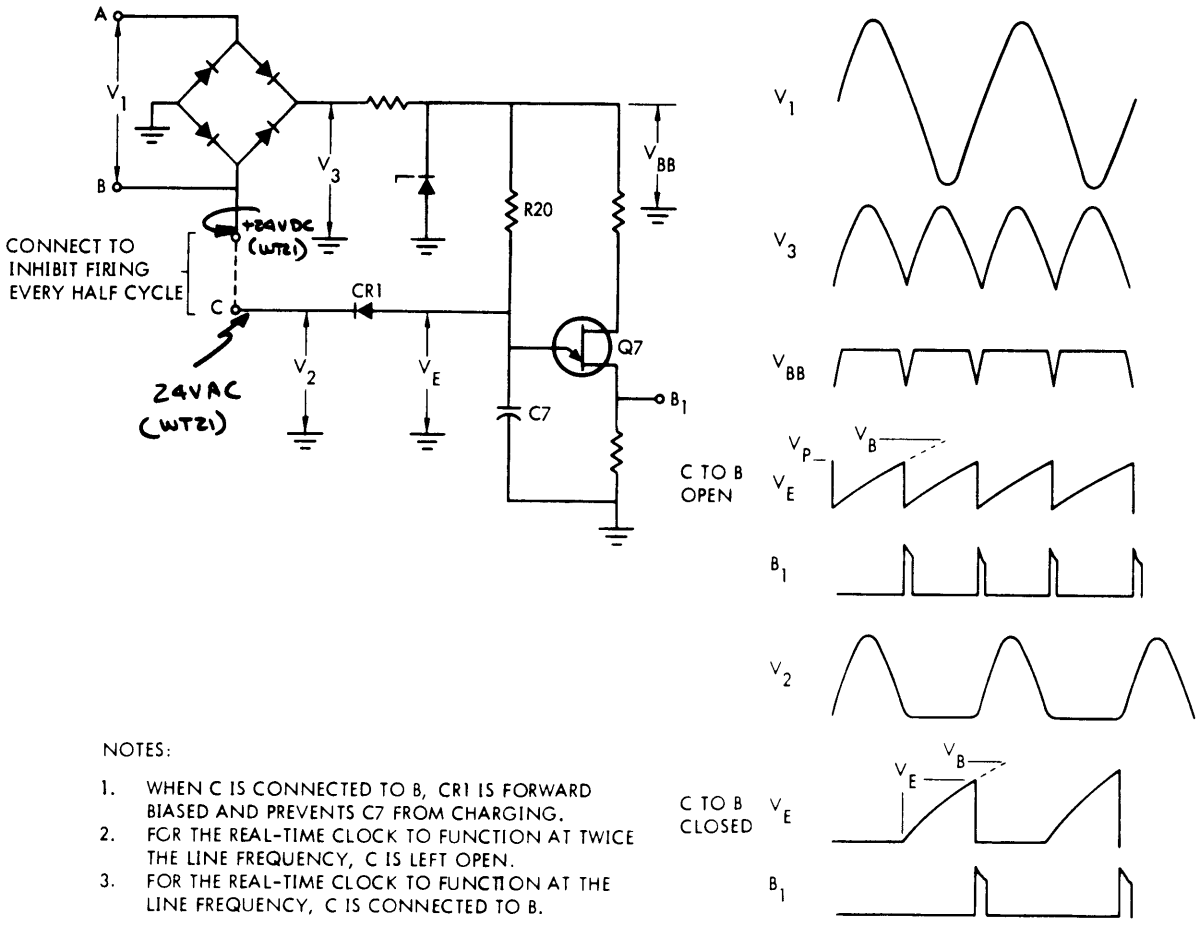


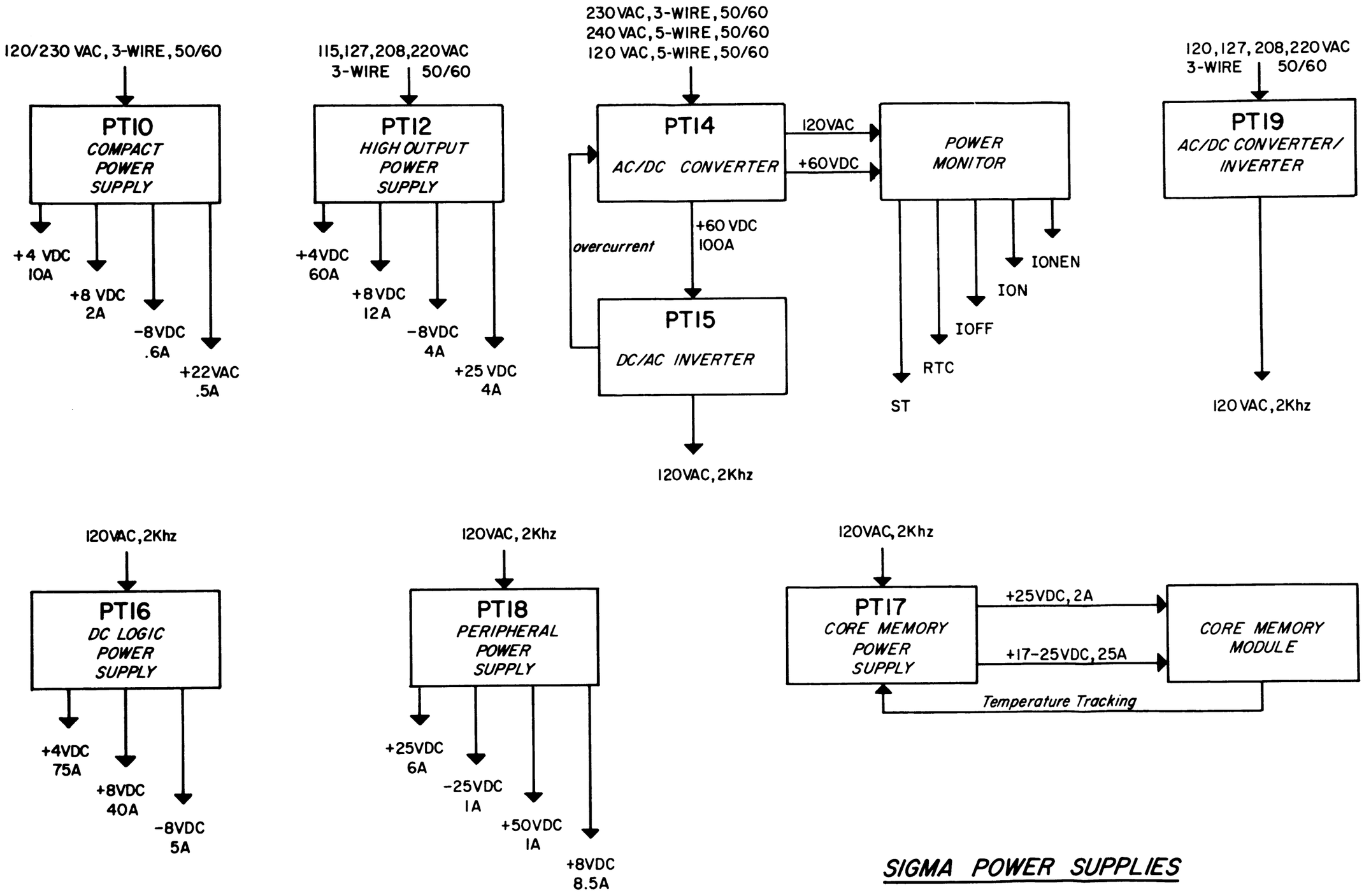
Figure 3-648. ION One-Shot Operation



NOTES:

1. WHEN C IS CONNECTED TO B, CR1 IS FORWARD BIASED AND PREVENTS C7 FROM CHARGING.
2. FOR THE REAL-TIME CLOCK TO FUNCTION AT TWICE THE LINE FREQUENCY, C IS LEFT OPEN.
3. FOR THE REAL-TIME CLOCK TO FUNCTION AT THE LINE FREQUENCY, C IS CONNECTED TO B.

Figure 3-649. Real-Time Clock Operation



SIGMA POWER SUPPLIES

POWER SUPPLY

MODELS PT14 PT15

GENERAL DESCRIPTION

1-1 INTRODUCTION

1-2 SCOPE OF MANUAL

1-3 This manual describes Power Supply Models PT-14 and PT-15 (figure 1-1), designed and manufactured by Scientific Data Systems, Santa Monica, California. This manual includes specifications, theory of operation, installation and maintenance procedures, performance testing and trouble analysis, parts lists, and drawings. To obtain the number and title of publications that contain data on related equipment refer to the List of Related Publications at the front of this manual.

1-4 PURPOSE OF EQUIPMENT

1-5 The PT-14/PT-15 power supply combination is used to convert 50 hz or 60 hz commercial power to 2000 hz for use in high frequency computer power distribution systems. The PT-14/PT-15 provides 120 vac, 2000 hz, 3600 volt-ampere to other computer power supplies. The PT-14 is an ac-dc converter, which converts 120/208 volts ac, 3-phase, 4-wire, 50 or 60 hz to 56 volts dc at 100 ampere. The PT-15 is a dc-ac inverter, which inverts the 56 volts dc to 120 volts ac at a frequency of 2000 hz and can supply 3600 volt-ampere to power supply loads. These power supply loads convert the 2000 hz to the various dc levels required for computer operation.

1-6 PHYSICAL DESCRIPTION

1-7 The PT-15 power supply is a solid-state type mounted on a steel chassis and equipped with a cooling fan. The dimensions are 22 inches by 13.9 inches by 7.75 inches. The PT-15 power supply is a solid-state type which has 3 printed circuit boards, a heat-sink chassis mounting power transistor, and a pair of cooling fans. The PT-14 dimensions are 22-1/2 inches by 21-1/2 inches by 7-3/4 inches.

1-8 FUNCTIONAL DESCRIPTION

1-9 The PT-14 and PT-15 (figure 1-2), operate in conjunction with each other. The power supplies use 45-66 cycle three-phase ac power to generate 2000 hz, 120 vac power. The PT-14 operates from three-phase primary power applied through a circuit breaker that can be tripped by either an over-current or over-temperature signal applied from the PT-15. The circuit breaker protects the equipment from over-current conditions and from over-heat conditions that might develop in the PT-15.

1-10 The three-phase primary power applied to the PT-14 is stepped down by the PT-14 power transformer and applied to a rectifier-filter circuit. The output of the PT-14 is 56 ± 9 vdc, 100 ampere. The output is unregulated, but highly filtered; 14 capacitors of large capacitance value enable sufficient energy storage to keep the output voltage within specified limits for 10 milliseconds after input power is removed.

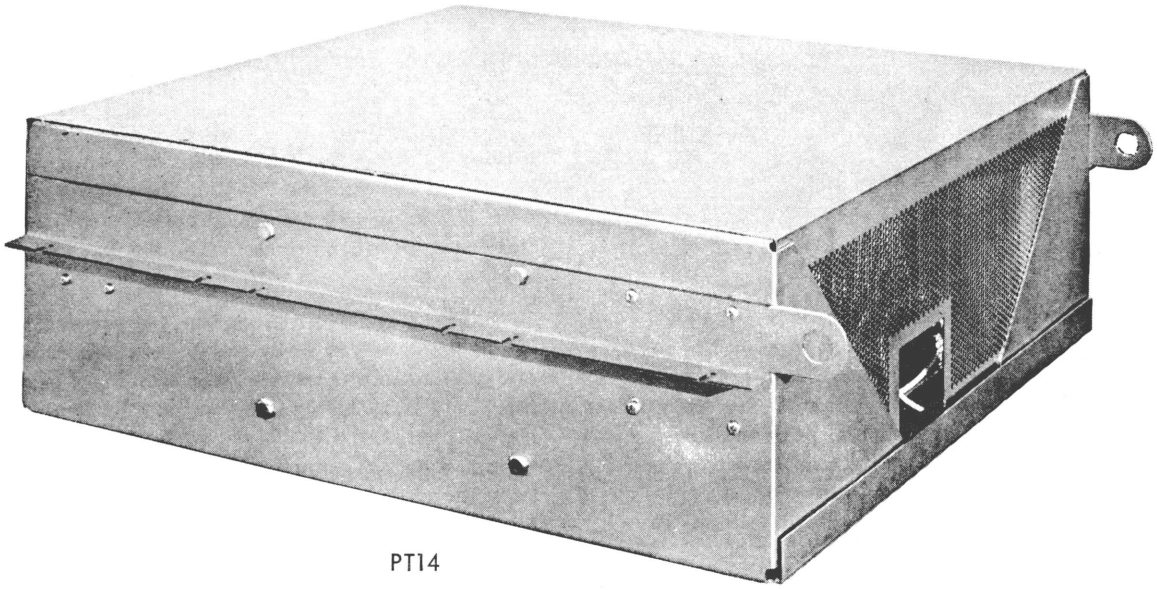
1-11 The PT-14 supplies the necessary 56 vdc power to drive the PT-15. The PT-15 is basically a square-wave transistor whose output is pulse-width modulated to obtain regulation. The output of a low-level saturable core, 2000 hz oscillator (WT10) is pulse-width modulated using a magnetic amplifier. The magnetic amplifier output is used to drive a switching transistor power amplifier stage, whose output is stepped up to provide the required 120 volts ac at 2000 hz.

1-12 The power transformer output current level is sensed by the output current transformer which supplies a feedback signal to the WT12 over-current control board. The WT12 board supplies over-current signals to trip the circuit breaker in the PT-14 when an over-current in excess of 125% of full load current exists. The thermal switch senses heat-sink temperature in the PT-15 and supplies a signal which trips the PT-14 circuit breaker when temperatures in excess of 135°C ± 10% occur.

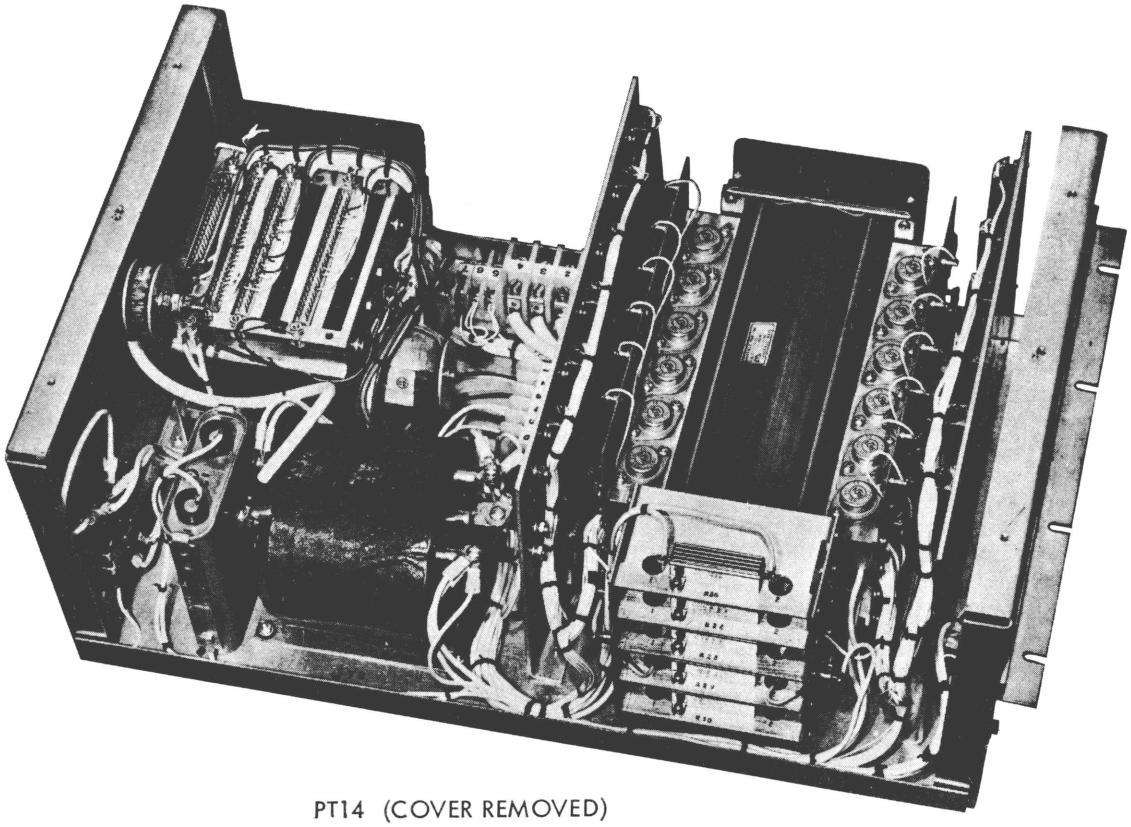
1-13 The WT11 control board senses the output voltage and provides control current for the magnetic amplifier. The magnetic amplifier controls the base current applied to the transistors of the power amplifier to achieve regulation. (See simplified schematic, figure 7-2.)

1-14 SPECIFICATIONS AND LEADING PARTICULARS

1-15 Tables 1-1 and 1-2 provide the essential specifications and leading particulars for the PT-14 and PT-15 respectively.

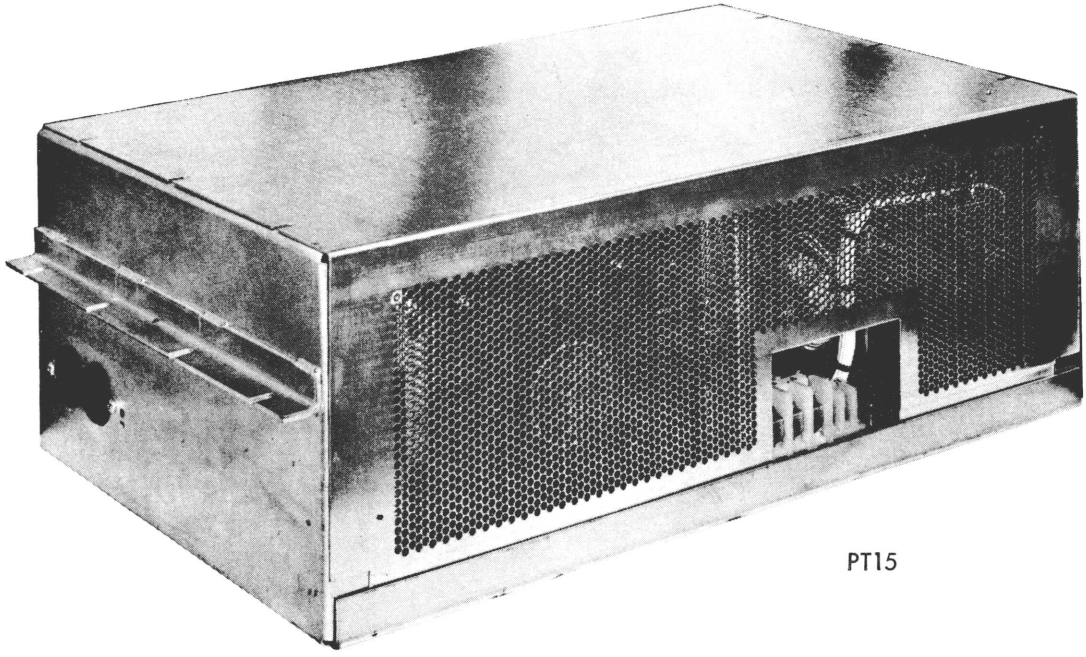


PT14

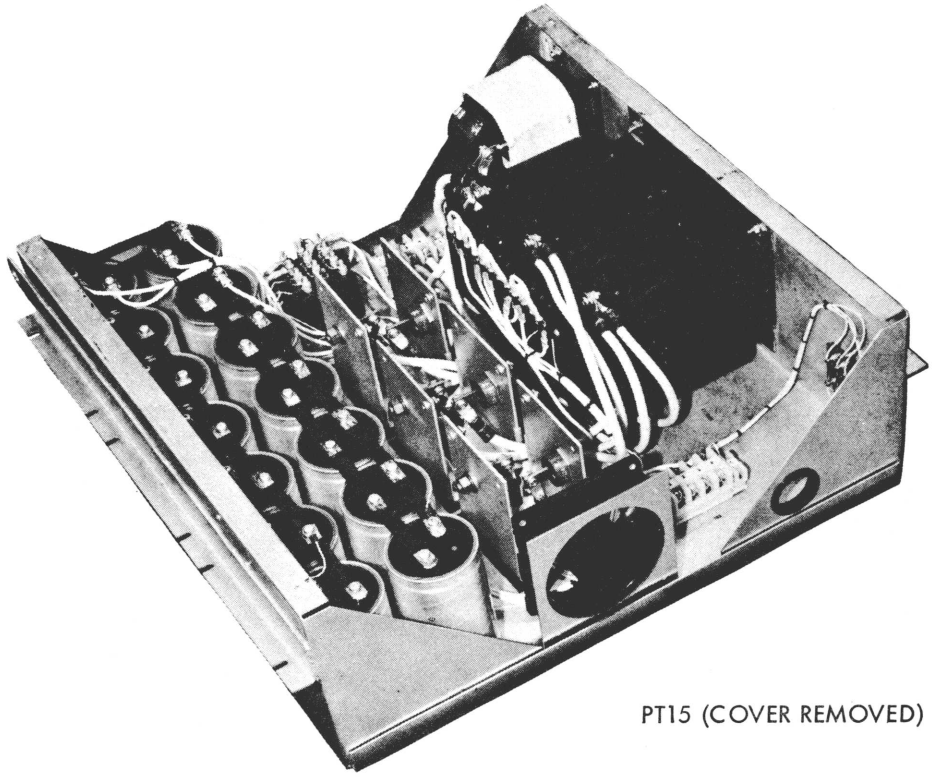


PT14 (COVER REMOVED)

Figure 1-1. PT-14/PT-15 Power Supply (Sheet 1 of 2)



PT15



PT15 (COVER REMOVED)

Figure 1-1. PT-14/PT-15 Power Supply (Sheet 2 of 2)

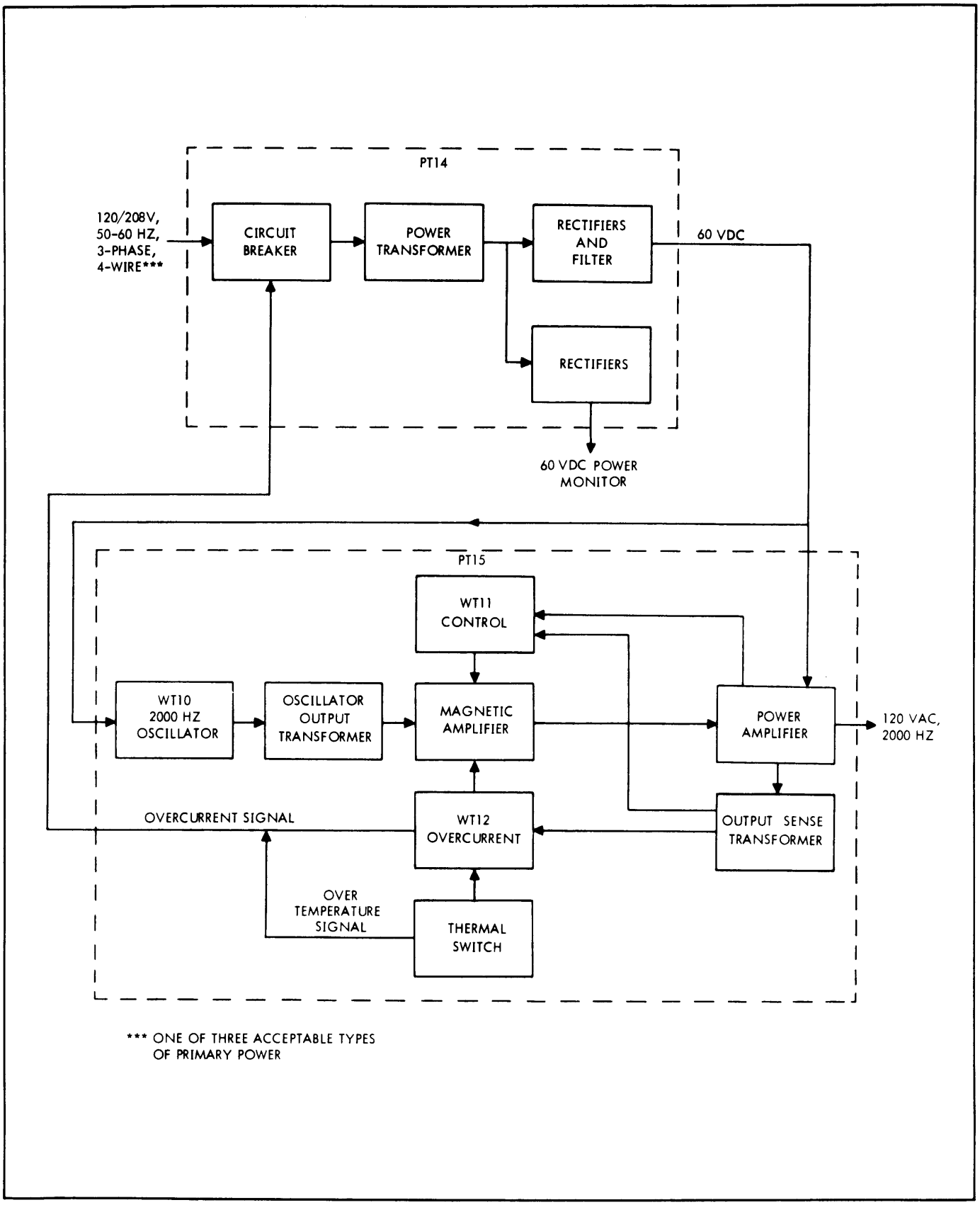


Figure 1-2. PT-14/PT-15 Power Supply Functional Block Diagram

Table 1-1. PT-14 Leading Particulars

Primary Power Requirements (one of three):	120/208 vac, 45-66 cycle, 3-phase, 4-wire 240/415 vac, 45-66 cycle, 3-phase, 4-wire 230 vac, 45-66 cycle, 3-phase, 3-wire
Output	+56 ± 9 vdc, 100 ampere
Power Consumption	6000 watts (maximum load)
Over-Voltage Protection	Circuit breaker that trips when over-current or over-heating occurs. Signal applied from PT-15
Operating Range	0° to 55° centigrade
Weight	115 pounds
Size:	
Length	22-1/2 inches
Width	24 inches
Depth	7-3/4 inches

Table 1-2. PT-15 Leading Particulars

Primary Power Requirements:	56 ± 9 vdc @ 100 ampere
Output	120 vac, single phase (fan power) 120 vac, 2000 hz ± 5% for all combinations of input/output variations at 50% load
Power Consumption	6000 watts (maximum load)
Over-Temperature Protection	Temperature switch that actuates at 135° centigrade ± 10% and trips circuit breaker which removes primary power from the PT-14 and PT-15
Operating Range	0° to 55° centigrade
Over-Current Protection	Printed circuit board WT12 sends over-current signal to circuit breaker CB1 which removes primary power from PT-14 and PT-15
Weight	35 pounds
Size:	
Length	13-1/2 inches
Width	24 inches
Depth	7-3/4 inches

OPERATION

2-1 INTRODUCTION

2-2 Operation consists of energizing and de-energizing the PT-14 and PT-15 power supplies. The PT-14 has no controls or adjustments other than circuit breaker CB1.

2-3 OPERATING INSTRUCTIONS

2-4 The following paragraphs provide turnon and turnoff procedures for the PT-14 and PT-15. The PT-15 receives primary power from the PT-14, therefore the PT-14 must be energized before energizing the PT-15.

2-5 ENERGIZING THE PT-14

2-6 Energize the PT-14 in accordance with the following instructions:

a. Connect primary power to terminal board TB3. Any one of three types of primary power is suitable, as shown in figure 7-1 and as explained in table 1-1.

b. Set circuit breaker CB1 to ON.

c. Check to see that muffin fan B1 is operating.

d. Using Simpson Model 269 VOM, check for presence of electrical power as indicated at the following terminal boards and pins:

Terminal Board Connection	Voltage Reading
TB1, pins 1 and 4	56 ± 9 vdc
TB1, pins 5 and 6	120 vac
TB3, pins 5 and 6	56 vdc ± 9 vdc

2-7 DE-ENERGIZING THE PT-14

2-8 De-energize the PT-14 by disconnecting primary power from terminal board TB3, or set circuit breaker CB1 to OFF.

2-9 ENERGIZING THE PT-15

2-10 Energize the PT-15 in accordance with the following instructions:

a. Connect PT-14 dc output power positive terminals to terminals 1 and 2 of PT-15 terminal board TB1.

b. Connect PT-14 dc output power negative terminals to terminals 3 and 4 of PT-15 terminal board TB1.

c. Connect 120 vac, single-phase power for operation of muffin fans B1 and B2 from terminals 5 and 6 of PT-14 terminal board TB1 to terminals 5 and 6 of PT-15 terminal board TB1. Check to see that fans operate.

d. Connect over-current signal lead from terminal 7 of TB1 (PT-15) to terminal 7 of TB1 (PT-14).

2-11 DE-ENERGIZING THE PT-15

2-12 Disconnect all power connections and signal connections between PT-14 and PT-15 in accordance with the following steps. To remove primary power only (leaving over-current signal connections and operating power for muffin fans B1 and B2) perform steps a and b only.

a. Disconnect positive dc power input lead from terminals 1 and 2 of TB1.

b. Disconnect negative dc power input lead from terminals 3 and 4 of TB1.

c. Disconnect 120 vac, single-phase operating power for muffin fans from terminals 5 and 6 of TB1.

d. Disconnect over-current signal lead from pin 7 of TB1.

POWER SUPPLY

MODEL PT16

SECTION I
GENERAL DESCRIPTION

1-1 INTRODUCTION

1-2 SCOPE OF MANUAL

1-3 This manual describes Power Supply Model PT16 that is designed and manufactured by Scientific Data Systems, Inc., Santa Monica, California. This manual includes a general description of the power supply, operating procedures, theory of operation, installation and maintenance procedures, performance testing and trouble analysis information, parts lists, and drawings. To obtain the number and title of publications that contain data on related equipment refer to the List of Related Publications at the front of this manual.

1-4 PURPOSE OF EQUIPMENT

1-5 The power supply provides regulated dc power at +4.2v, -8v, and +8.4v. It operates from 120v, 2000-hz power supplied by inverters (PT19 or PT14/PT15 combination). The List of Related Publications lists the technical manuals for various equipment in which the power supply is installed.

1-6 PHYSICAL DESCRIPTION

1-7 The power supply (figure 1-1) is a solid-state type with component parts mounted on a steel chassis. It contains one printed circuit board. A 6-foot cable fitted with a three-pin polarized connector connects primary power from the inverter to the power supply. Another cable fitted with a three-pin polarized connector connects primary power at 120v, 60-hz to operate a blower motor which is mounted on the chassis. The dimensions and weight of the power supply are given in table 1-1.

1-8 FUNCTIONAL DESCRIPTION

1-9 The power supply (figure 1-2) receives primary power at 120v, 2000-hz from either the PT15 or the PT19 power supply. It processes this input and provides outputs of +4.2v +8.4v, and -8v.

1-10 SPECIFICATIONS AND LEADING PARTICULARS

1-11 Table 1-1 provides the essential specifications and leading particulars pertaining to the power supply. Table 1-2 provides a fuse complement.

Table 1-1. Leading Particulars

Item	Specification
Primary power	120v (±5%), 2000 (±200) hz, 15 amp square wave
Fan power	120v, 60 hz, 0.2 amp
Outputs	+4.2 (±0.2)v, 75 amp, with 0.2v (max) peak-to-peak ripple +8.40 (±0.42)v, 40 amp, with 0.4v (max) peak-to-peak ripple -8.0 (±0.5)v, 5 amp, with 0.56v (max) peak-to-peak ripple
Power output	660w (maximum load)
Overvoltage protection	Primary power removed at 50% overvoltage on +4v and +8v outputs only for most conditions
Temperature range:	
Operating	0° to 55°C (32° to 131°F)
Nonoperating	-20° to 85°C (68° to 185°F)
Dimensions	22.5 x 5.5 x 5.5 in.
Weight	33 lb

Table 1-2. Fuse Complement

Reference Designator	Type	Rating	Location	Quantity
F1	3 AG	125v, 8 amp	Fuse mounting bracket	1
F2	3 AG	125v, 8 amp	Fuse mounting bracket	1
F3	3 AG	125v, 8 amp	Fuse mounting bracket	1

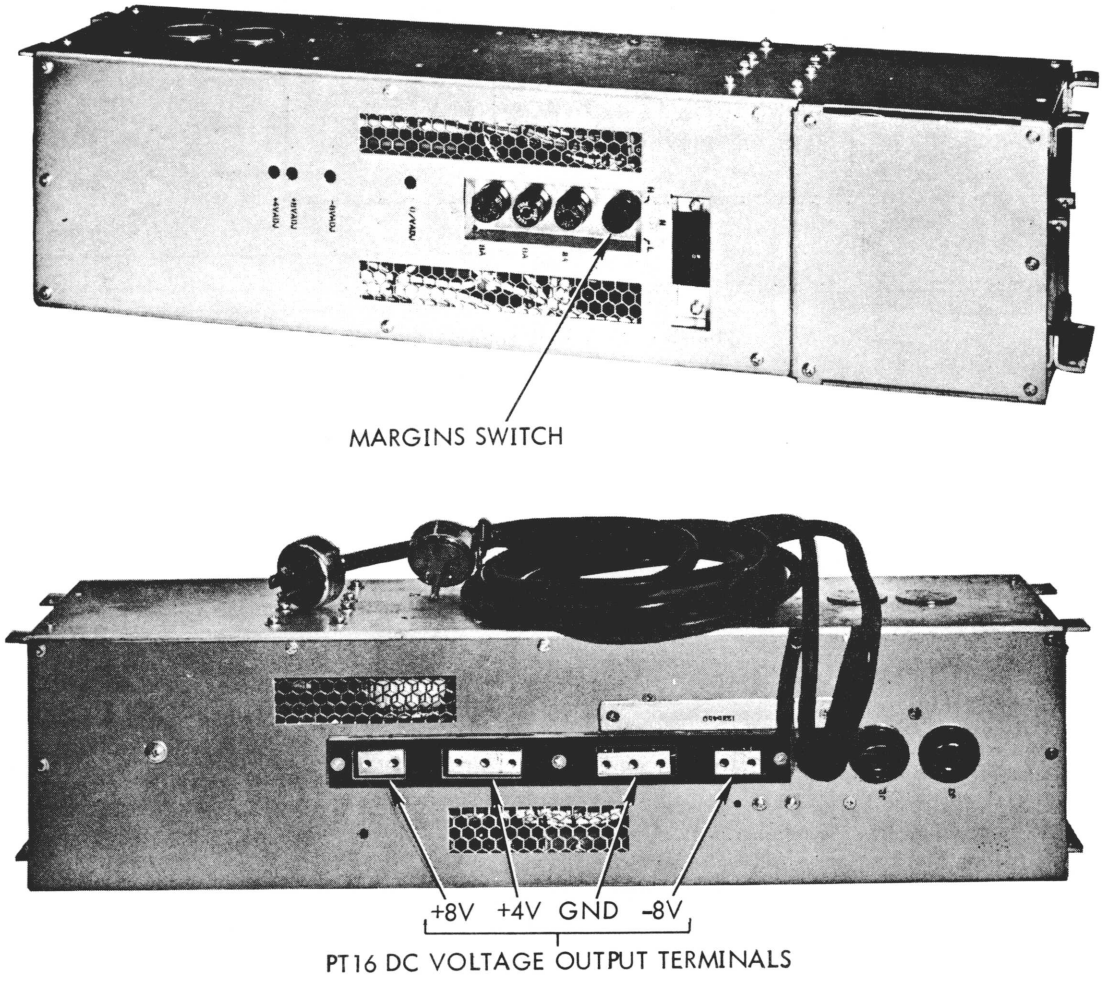


Figure 1-1. Power Supply Model PT16

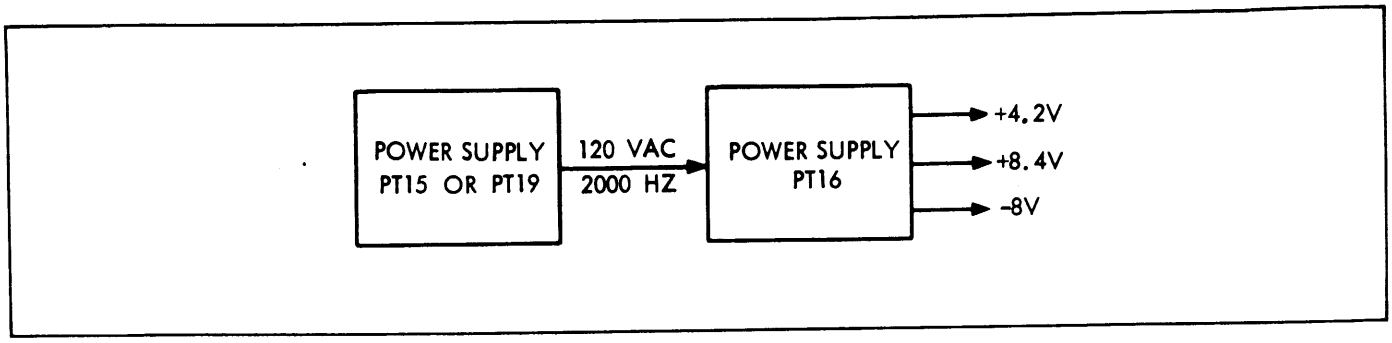


Figure 1-2. Power Supply, Block Diagram

SECTION II

OPERATION

2-1 INTRODUCTION

2-2 This section provides a list of controls and adjustments as well as operating instructions for the power supply.

2-3 CONTROLS AND ADJUSTMENTS

2-4 Table 2-1 lists the controls and adjustments for the power supply and gives a brief explanation of their function. The location of the controls and adjustments is shown in figure 1-1.

Table 2-1. Controls and Adjustments

Control or Adjustment	Reference Designator	Function
O/V ADJ potentiometer	R3	Adjusts point at which circuit breaker CB1 trips by setting bias voltage level at base of transistor Q1 in overvoltage protection circuit
+4V ADJ potentiometer	R12	Adjusts +4.2v output to correct level
+8V ADJ potentiometer	R18	Adjusts +8.4v output to correct level
-8V ADJ potentiometer	R22	Adjusts -8v output to correct level
Margins switch (H-N-L)	S1	Provides means of performing marginal testing of Sigma equipment by changing +4.2v, +8.4v, and -8v outputs to a higher or lower level. With the switch in the N (normal) position, outputs are set for normal level. With the switch in low (L) position, the outputs will be +3.6v,

Table 2-1. Controls and Adjustments (Cont.)

Control or Adjustment	Reference Designator	Function
Margins switch (H-N-L) (Cont.)		-3.6v, and +7.2v, (+0, -2%). With the switch in high (H) position the outputs will be +4.4v, +8.8v, and -8.8v (+0, -2%)

2-5 OPERATING INSTRUCTIONS

2-6 ENERGIZING THE POWER SUPPLY

2-7 Energize the power supply as follows:

a. Set margins switch S1 to N (normal).

b. Set circuit breaker CB1 to ON.

2-8 DEENERGIZING THE POWER SUPPLY

2-9 To deenergize the power supply, set circuit breaker CB1 to OFF.

2-10 POSITIONING THE MARGINS SWITCH

2-11 The margins switch (S1) has positions of H (high), N (normal), and L (low). The margins switch provides test capability by supplying voltages of a marginal level (±10 percent of normal level) to the Sigma logic circuits.

2-12 Marginal testing is accomplished as follows:

a. To supply an operating voltage 10 percent below normal, position margins switch to L.

b. To supply an operating voltage 10 percent above normal, position margins switch to H.

2-13 For normal operation of the power supply the margins switch should be set to N.

POWER SUPPLY

MODEL PT17

SECTION I
GENERAL DESCRIPTION

1-1 INTRODUCTION

1-2 SCOPE OF MANUAL

1-3 This manual describes Power Supply Model PT-17 (figure 1-1) designed and manufactured by Scientific Data Systems, Inc., Santa Monica, California. Contents of this manual include specifications, theory of operation, installation and maintenance procedures, performance testing and trouble analysis, parts lists, parts location drawings, schematics, and an installation drawing. To obtain the number and title of publications that contain data on related equipment refer to the List of Related Publications at the front of this manual.

1-4 PURPOSE OF EQUIPMENT

1-5 The power supply provides two regulated voltage outputs to the Sigma memory units. There is an internal overload protection which consists of a circuit breaker and fuses. This system may be tripped by logic signals from the memory unit, power supply dropout or overload.

1-6 PHYSICAL DESCRIPTION

1-7 The power supply is solid-state, mounted on a cadmium-plated steel chassis, and is equipped with a cooling fan. The assembly includes two printed circuit modules. Two 72-inch power cables receive primary power for the supply and the cooling fan. The power supply weighs 40 pounds, is 27.75 inches long, 6.5 inches high, and 6.56 inches deep.

1-8 FUNCTIONAL DESCRIPTION

1-9 The power supply (figure 1-2) operates from primary power received from the PT-14/PT-15 inverter. Two regulated voltage outputs (+25 vdc, 0-20 amperes (V_E) +25 vdc, 0-2 amperes (V_D) may be adjusted between +18 and +25 volts by switches on the PT-17. Two printed circuit modules provide regulation and protection for the supply. A feedback loop from the Sigma memory unit enables the power supply to be disconnected from primary power in the event of overtemperature. The output voltage of the variable output (V_D) has a temperature tracking circuit. This circuit varies V_D voltage output according to the temperature of the memory.

1-10 SPECIFICATIONS AND LEADING PARTICULARS

1-11 Table 1-1 provides essential specifications and leading particulars pertaining to the power supply. Table 1-2 provides a fuse complement.

Table 1-1. Leading Particulars

Item	Specification
Power requirements	
Primary input power	120 (±6) v, 2000 hz, 7 amp
Fan power	115v, 47-63 hz, 0.2 amp
Output voltages and current	
Adjustable (V_D)	+25v (17-25) ± 1%, 0 to 20 amp (static), 0 to 25 amp (dynamic)
Nonadjustable (V_C)	+25v ± 1%, 0 to 2 amp

Table 1-1. Leading Particulars (Cont.)

Item	Specification
Temperature tracking	The adjustable output changes -120 mv for every degree of temperature rise in memory unit. A zero adjustment feature enables adjustment of initial output voltage at ambient temperature
Overload protection	Circuit breaker and temperature switches provide overvoltage, overcurrent, and overtemperature protection. Overvoltage protection is adjustable between +25-30 vdc Overcurrent feature operates at 25 to 50% over (nominal) maximum current output Circuit breaker can also be triggered by +4v logic signal from memory unit
Operating temperatures	
Operating	0° to 55° C
Nonoperating	-20° to 85° C
Weight	40 lb
Supply internal impedance	
+25v adjustable	1.25 ohms
+25v nonadjustable	12.5 ohms
Dimensions	
Length	27.75 in.
Height	6.5 in.
Depth	6.56 in.

Table 1-2. Fuse Complement

Reference Designator	Type	Rating	Location	Quantity
F1	Bussman ABC series, 3AG	15 amp 250v	Adjacent to circuit breaker CB1 on side of power supply	1

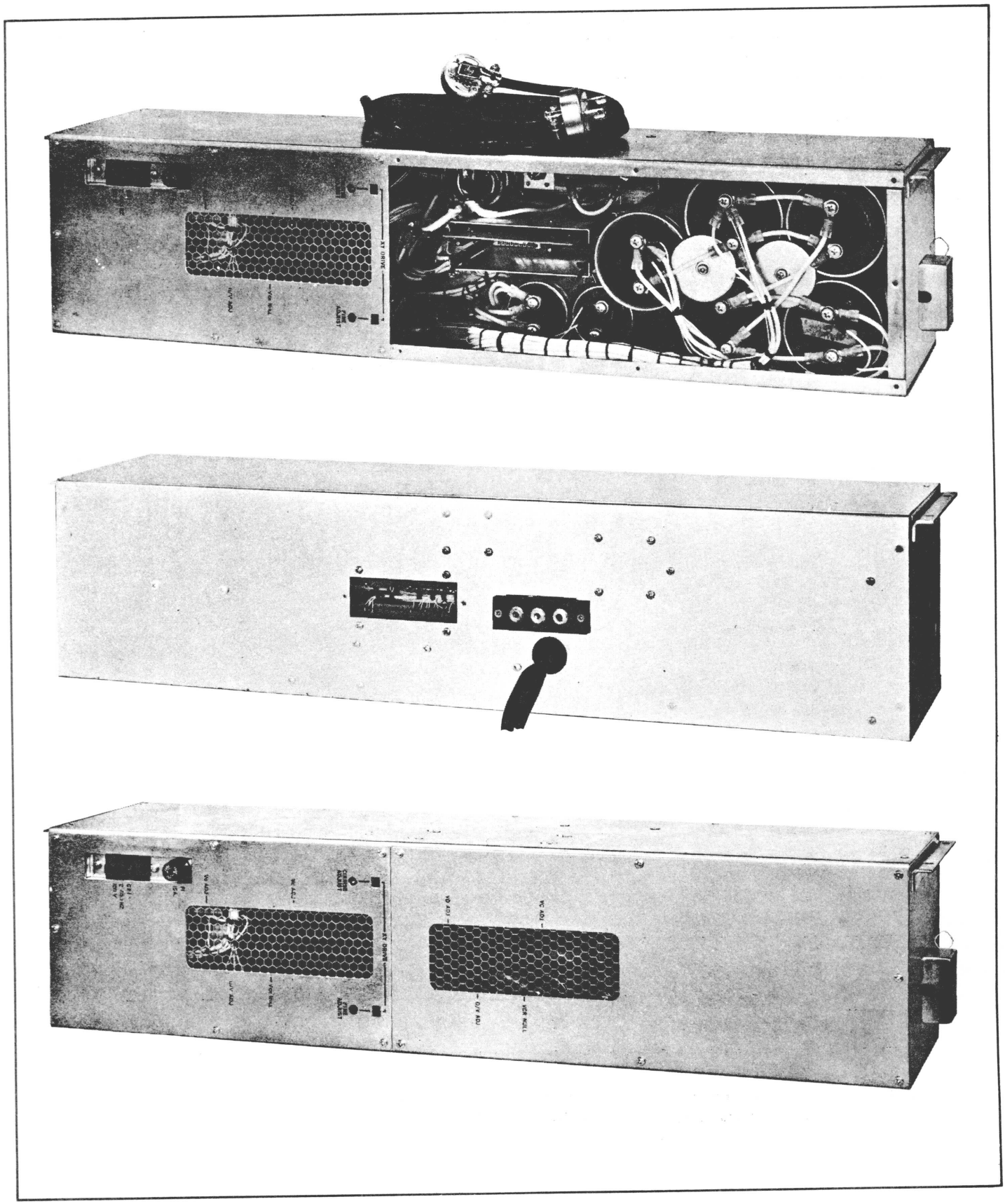


Figure 1-1. Power Supply

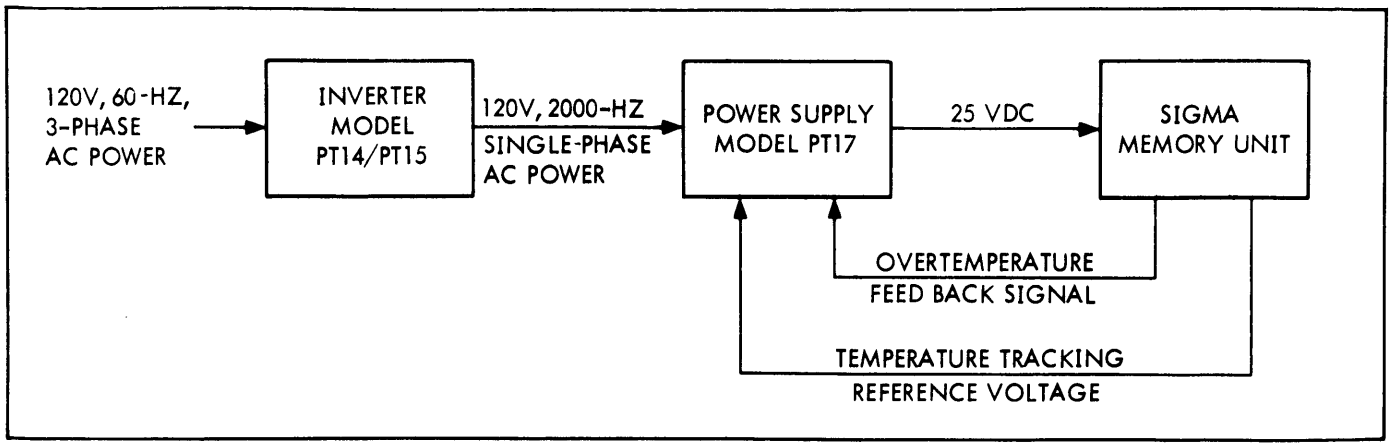


Figure 1-2. Functional Block Diagram

SECTION II
OPERATION

2-1 INTRODUCTION

2-2 This section provides operating instructions and a list of controls and adjustments for the power supply.

2-3 CONTROLS AND INDICATORS

2-4 Table 2-1 provides a list of controls and adjustments. The circuit breaker and switches are located on the power supply cover plate. The potentiometers are located on voltage regulator printed circuit modules WT-14 and WT-15. Figure 1-1 illustrates the controls and adjustments.

2-5 OPERATING INSTRUCTIONS

2-6 Operating instructions include procedural steps for energizing and deenergizing the power supply, and for setting the COARSE ADJUST and FINE ADJUST switches S1 and S2.

2-7 ENERGIZING THE POWER SUPPLY

2-8 Energize as follows:

a. Check that primary power is applied to PT-14/PT-15 inverter.

b. Set circuit breaker CB1 on power supply to OFF.

Table 2-1. Controls and Adjustments

Name	Reference Designator	Function
400 hz, 120v	CB1	Applies primary power to the power supply
COARSE ADJUST	S1	Divides V_{R2} voltage to provide reference voltage to WT-14 regulator module to control V_D output. Switch has active positions of 0 through 9 and position R which is inactive
FINE ADJUST	S2	Divides output of COARSE ADJUST switch S1 to control V_D output. Switch has active positions 0 through 9 and position R which is inactive
V_D ADJ	R6 (WT-14)	Adjusts level of reference voltage supplied to FINE ADJUST switch
V_{CR} NULL	R6 (WT-15)	Adjusts level of voltage (V_{CR}) applied to base of transistor stage Q3. Enables adjustment of Sigma memory temperature reference voltage
V_C ADJ	R25 (WT-14)	Adjusts level of V_C feedback voltage applied to base of differential amplifier stage Q8. This provides adjustment for power supply +25 vdc V_C output
O/V ADJ	R26 (WT-15)	Adjusts level of emitter bias voltage (V_E) at unijunction transistor stage Q7. This adjustment enables setting of firing level of protection circuit

c. Connect plug P2 power cable to 120-vac, 60-hz power.

d. Connect plug P1 on power cable to mating power receptacle on PT-14/PT-15 inverter.

e. Set circuit breaker CB1 to ON.

f. Check that blower motor operates.

2-9 DEENERGIZING THE POWER SUPPLY

2-10 Deenergize as follows:

a. Set circuit breaker CB1 to OFF.

b. Disconnect plug P2 on power cable from 120-vac power.

c. Disconnect plug P1 on cable from PT-14/PT-15 inverter.

2-11 POSITIONING COARSE ADJUST AND FINE ADJUST SWITCHES

2-12 The COARSE ADJUST and FINE ADJUST switches S1 and S2 may be set to vary power supply output V_D which is available at the supply terminal block TB1, terminal 3. Set switches as follows:

a. To obtain a V_D output of +25v, set COARSE ADJUST and FINE ADJUST switches to 9.

b. To obtain a V_D output of +18v, set COARSE ADJUST and FINE ADJUST switches to 0.

c. To obtain a voltage output between +18v and +25v, first set COARSE ADJUST switch to various positions until a voltage slightly higher than desired level is obtained. Set FINE ADJUST switch to obtain exact voltage.

POWER SUPPLY

MODEL PT18

SECTION I
GENERAL DESCRIPTION

1-1 INTRODUCTION

1-2 SCOPE OF MANUAL

1-3 This manual describes Power Supply Model PT-18 (figure 1-1), which is designed and manufactured by Scientific Data Systems, Santa Monica, California. This manual includes specifications, theory of operation, installation and maintenance procedures, performance testing and trouble analysis, a parts list, and drawings. To obtain the number and title of publications that contain data on related equipment, refer to the List of Related Publications at the front of this manual.

1-4 PURPOSE OF EQUIPMENT

1-5 The PT-18 provides regulated dc power at +8, -25, +25, and +50 volt levels. It operates from 120 vac, 2000 cycle power supplied by inverters (PT-19 or the PT-14/PT-15 combination). The List of Related Publications lists the equipment with which the PT-18 is related.

1-6 PHYSICAL DESCRIPTION

1-7 The PT-18 is mounted on a metal chassis and is enclosed with a ventilated cover. Its dimensions are 5.5 inches by 5.5 inches by 14.5 inches; its weight is 17 pounds. A six foot power cable fitted with a three-pin polarized connector connects primary power from the inverter to the PT-18.

1-8 FUNCTIONAL DESCRIPTION

1-9 The PT-18 provides regulated dc power at +50, +25, -25, and +8 volt levels (figure 1-2). The magnetic amplifier supplies regulated ac power to the two power transformers at a power level determined by the saturation state of the magnetic amplifier. The magnetic amplifier saturation state is controlled by the regulator circuit. Each dc output is supplied from a separate dc power (rectifier-filter) circuit. The feedback loop for ac input regulation is taken from the +25 volt output at a point past the output filter circuit. The PT-18 is therefore line regulated.

1-10 SPECIFICATIONS AND LEADING PARTICULARS

1-11 Table 1-1 provides the essential specifications and leading particulars of the PT-18. Table 1-2 lists the fuse complement.

Table 1-1. Leading Particulars

Primary Power Requirements	120 ± 12 volts ac, 2000 ± 200 cycles, @ 5 amperes
Outputs	+8 volts dc @ 8.5 amperes +25 volts dc @ 6.0 amperes -25 volts dc @ 1.0 amperes +50 volts dc @ 1.0 amperes
Power Consumption	480 watts under maximum load
Line Regulation	± 1%
Load Regulation	12%, minimum to maximum load
Ripple	2% maximum peak to peak
Drift	1% maximum
Voltage Adjustment	10% from normal resolution to within 2%
Operating Range	0° to 50° centigrade
Size	5.5 x 5.5 x 14.5 inches
Weight	17 pounds
Transient Recovery Time (minimum to maximum load)	500 milliseconds

Table 1-2. Fuse Complement

Reference Designator	Type	Rating	Location	Quantity
F1	3AG	250 volt 4.0 ampere	Control mounting bracket	1
F2	3AG	32 volt 7.5 ampere	Control mounting bracket	1
F3, F5	3AG	250 volt 1.5 ampere	Control mounting bracket	2
F4	3AG	32 volt 10.0 ampere	Control mounting bracket	1

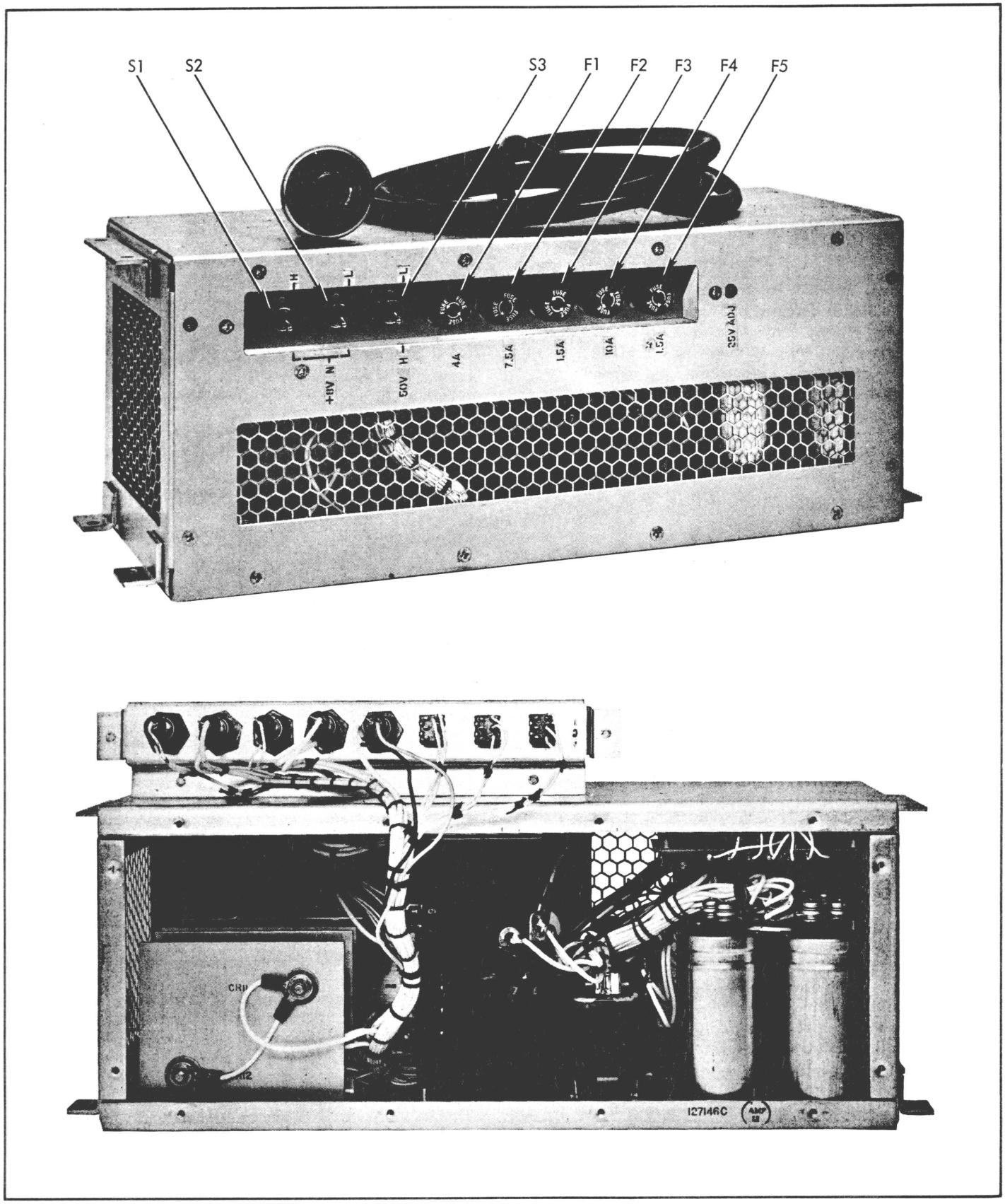


Figure 1-1. Power Supply Model PT-18

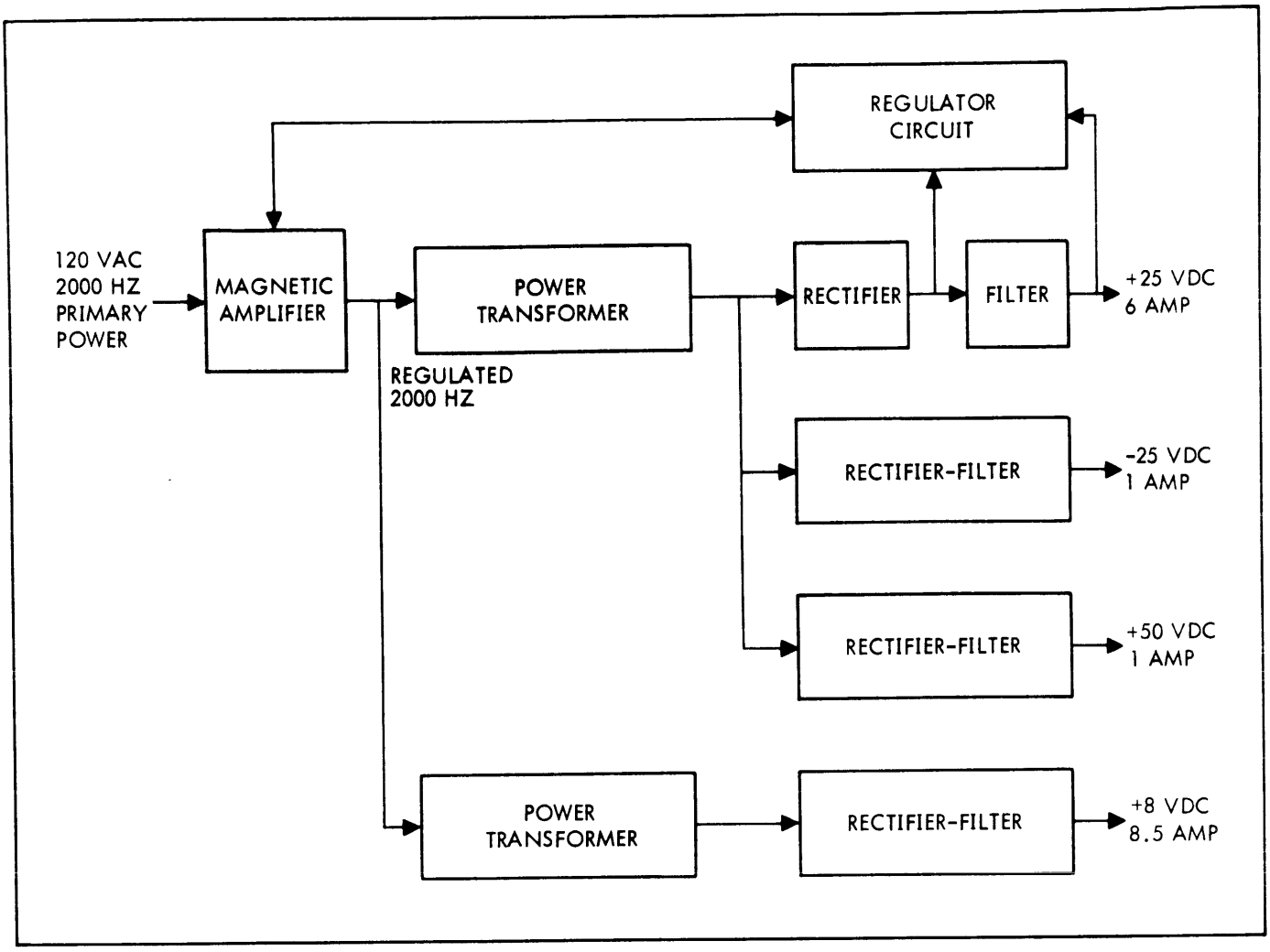


Figure 1-2. Power Supply Model PT-18 Functional Block Diagram

SECTION II
OPERATING

2-1 INTRODUCTION

2-2 This section provides a list of controls, adjustments, and operating instructions for the PT-18.

2-3 CONTROLS AND ADJUSTMENTS

2-4 Table 2-1 lists the controls and adjustments on the PT-18; figure 1-1 shows the controls and adjustments.

Table 2-1. Controls and Adjustments

Name	Reference Designator	Function
+8V (Upper) N-H	S1	Adjusts +8v output voltage 10% higher when set to H
+8V (Lower) N-L	S2	Adjusts output voltage 10% lower when switch set to L
50V H-L	S3	Adjusts +50 volt output 10% higher when set to H
25V ADJ	R2	Adjusts all output voltages ± 10%, but normally is used to set +25 volt output. Both +8v switches and the 50v switch should be set to N for this adjustment

2-5 OPERATING INSTRUCTIONS

2-6 ENERGIZING THE PT-18

2-7 Energize the PT-18 as follows:

a. Check to see that primary power is applied to associated inverter (PT-19 or PT-14/PT-15 combination).

b. Connect plug P1 on PT-18 primary power cable into mating primary power receptacle on inverter.

c. Using Simpson 269 multimeter, test for the following power output levels at terminal board TB1 terminals:

TB1 Terminals	Required Voltage Levels
+8 8.5A	+8 vdc ± 0.4 vdc
+25 6A	+25 vdc ± 1.0 vdc
-25 1A	-25 vdc ± 1.6 vdc
+50 1A	+50 vdc ± 2.5 vdc

2-8 DE-ENERGIZING THE PT-18

2-9 De-energize the PT-18 by removing the power cable from the primary power receptacle on the inverter.

POWER SUPPLY

MODEL PT19

SECTION I
GENERAL DESCRIPTION

1-1 INTRODUCTION

1-2 SCOPE OF MANUAL

1-3 This manual describes Power Supply Model PT19, designed and manufactured by Scientific Data Systems, Santa Monica, California. This manual includes a general description, theory of operation, installation and maintenance procedures, performance testing and trouble analysis, parts lists, and drawings. To obtain the number and title of publications that contain data on related equipment, refer to the List of Related Publications at the front of this manual.

1-4 PURPOSE OF EQUIPMENT

1-5 The PT19 power supply supplies 120-vac, 2000-hz power which, when connected,can utilize any one of four types of primary power: 120 vac, 127 vac, 208 vac, or 220 vac. It is normally connected for 120 volt operation.

1-6 PHYSICAL DESCRIPTION

1-7 The power supply (figure 1-1) is a solid-state type, mounted on a steel chassis. Primary power is received through a terminal board that is mounted on the chassis. Power is supplied through two power connectors (female receptacles) on the chassis. A heat sink and two blower fans are employed to maintain the eight power transistors in the supply at proper operating temperatures.

1-8 FUNCTIONAL DESCRIPTION

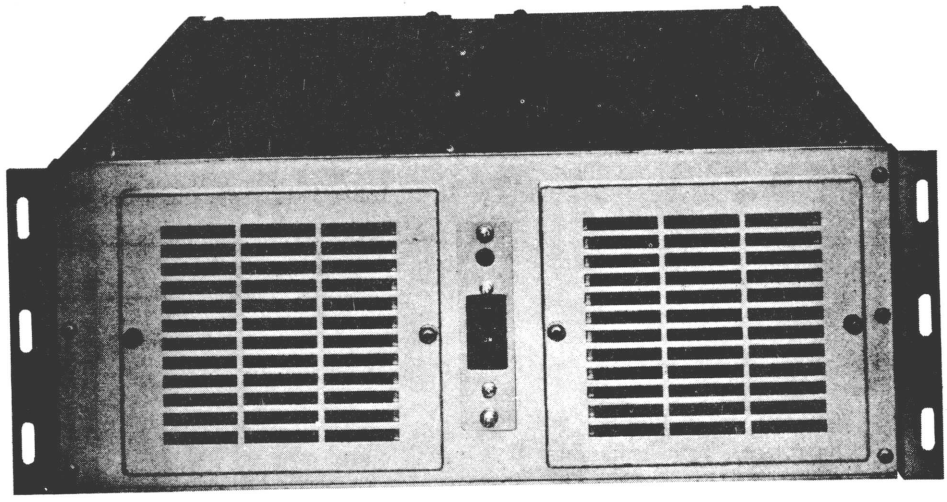
1-9 The PT19 power supply supplies 120-vac, 2000-hz power to other Sigma power supplies, including the PT16 and PT18. A functional block diagram is given in section III (figure 3-1).

1-10 SPECIFICATIONS AND LEADING PARTICULARS

1-11 Table 1-1 provides the essential specifications and leading particulars for the PT19 power supply. Table 1-2 provides the fuse complement.

Table 1-1. Specifications and Leading Particulars

Characteristics	Specifications
Primary power requirements (one of four):	120 (±10%) vac, single-phase, 47-63 hz, 23 amp 127 (±10%) vac, single-phase, 47-63 hz, 23 amp 208 (±10%) vac, single-phase, 47-63 hz, 23 amp 220 (±10%) vac, single-phase, 47-63 hz, 23 amp
Output:	120 (±10%) vac, 2000 (±5%) hz modified square wave at 1.2 kva
Overtemperature protection:	Overtemperature switch
Overcurrent protection:	Primary power removed by circuit breaker at 150% overload (most load conditions)
Cooling:	Two muffin fans with cooling air volume of 100 cfm
Temperature range:	
Operating	0°C to 55°C (32°to 131°F)
Nonoperating	-20°C to 85°C (68° to 185°F)
Weight:	101 pounds
Size:	
Length	18.94 inches
Width	19.06 inches
Height	6.82 inches



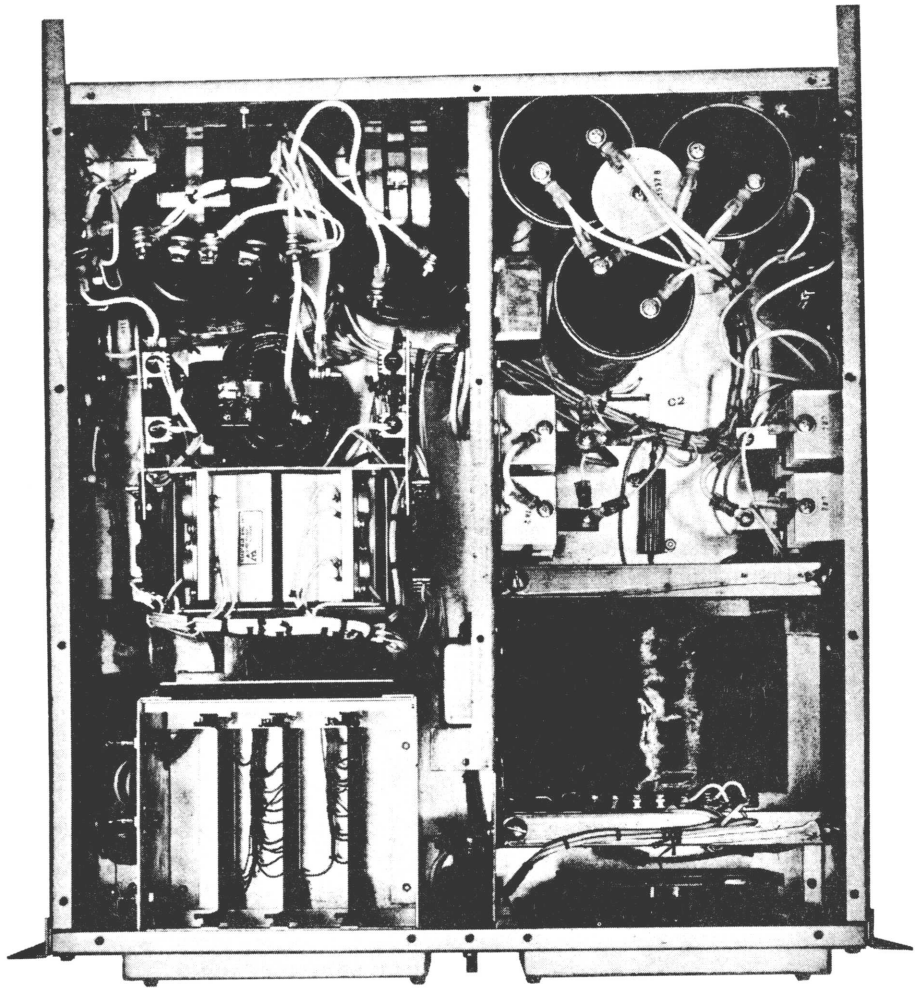


Figure 1-1. Power Supply Model PT19, Front and Top View

SECTION II
OPERATION

2-1 INTRODUCTION

2-2 Operation consists of energizing and deenergizing the power supply. The power supply has no controls other than circuit breaker CB1.

2-3 TURN-ON PROCEDURE

2-4 Energize the power supply as follows:

a. Ensure that primary power is connected to supply

b. Set circuit breaker CB1 to ON.

2-5 TURN-OFF PROCEDURE

2-6 Deenergize the power supply by setting circuit breaker CB1 to OFF.